Ordering number:ENN5169

Thick Film Hybrid IC

STK391-020

2-Channel Convergence Correction Circuit (I_C max = 6A)

Overview

The STK391-020 is a convergence correction circuit IC for video projectors. It incorporates two output amplifiers in a single package, making possible the construction of CRT horizontal and vertical convergence correction output circuits for each of the RGB colors using ust three hybrid ICs.

Applications

• Video projectors

Features

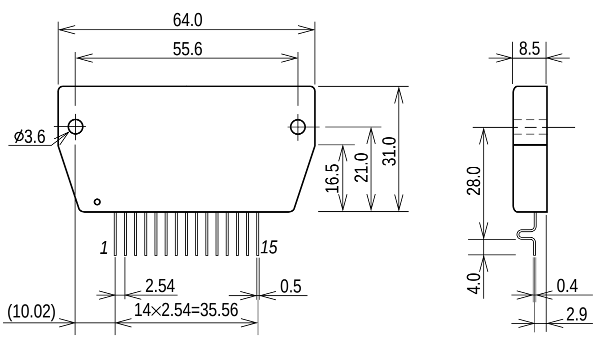
• 2 output amplifier circuits in a single package
• High maximum supply voltage (V_{CC} max = ±44V)
• Low thermal resistance (θj-c=2.7°C/W)
• High temperature stability (good idling current temperature compensation)
• Low correction coil inductance for improved oscillator stability (up to f_H = 64kHz)
• Pin compatible with the STK4274 for easy replacement

Package Dimensions

unit:mm

4062

[STK391-020]



SANYO : SIP15

Specifications

Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		±44	V
Maximum collector current	I_C	Tr9, 11, 20, 22	6.0	A
Thermal resistance	θ j-c	Tr9, 11, 20, 22 (per transistor)	2.7	˚C/W
Junction temperature	Tj		150	˚C
Operating temperature	Tc		105	˚C
Storage temperature	Tstg		–30 to +105	˚C

Operating Characteristics at Ta = 25˚C, Rg=50Ω, V_{CC}=±24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output noise voltage	V_{NO}				0.2	mVrms
Quiescent current	I_{CCO}			20	40	mA
Neutral voltage	V_N		–50	0	+50	mV
Output delay time	t_D	f=15.75kHz, triangular wave input, V_{OUT}=1.5Vp-p			1	µs

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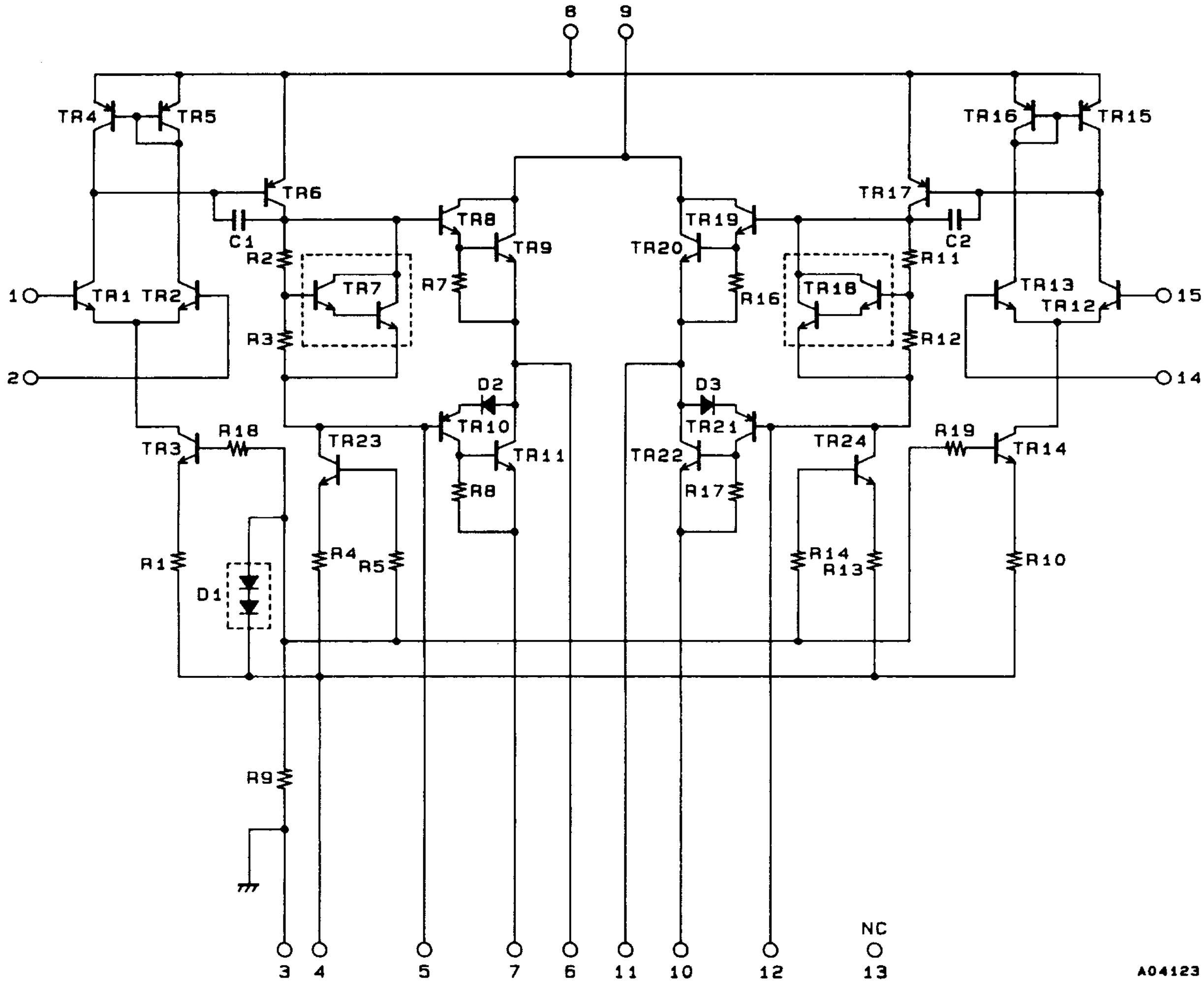
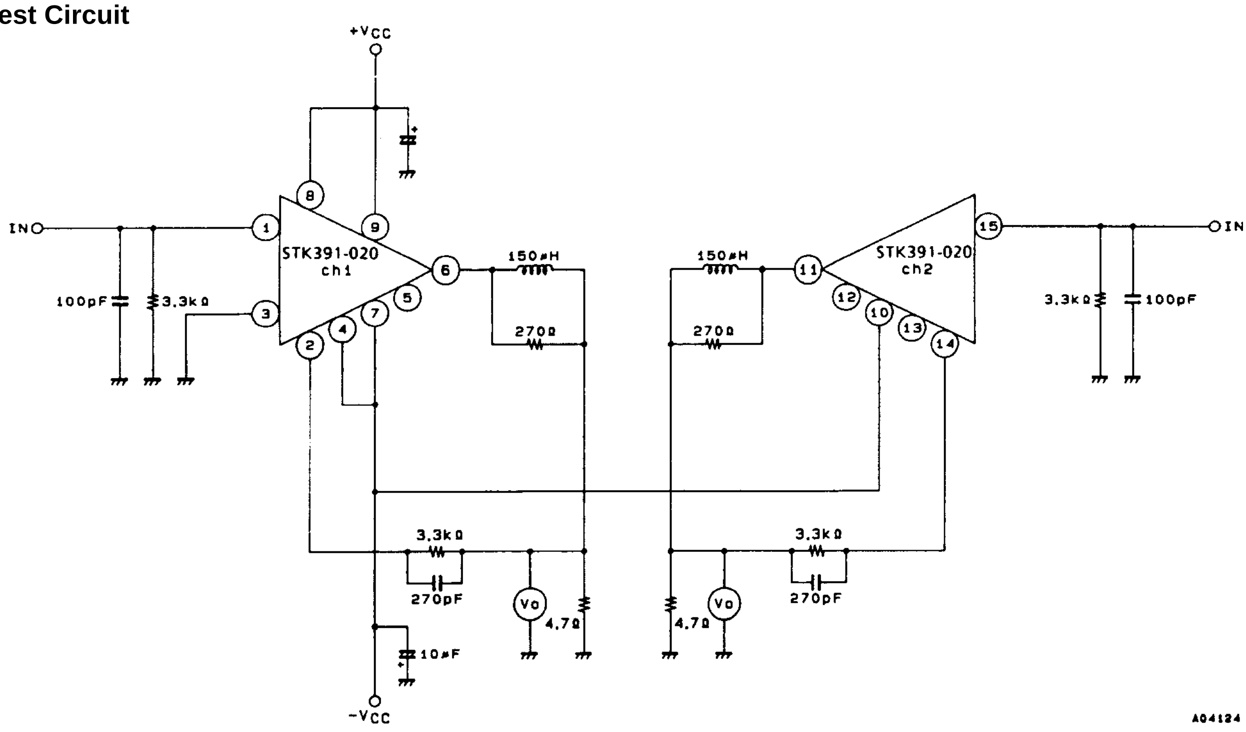
Equivalent Circuit

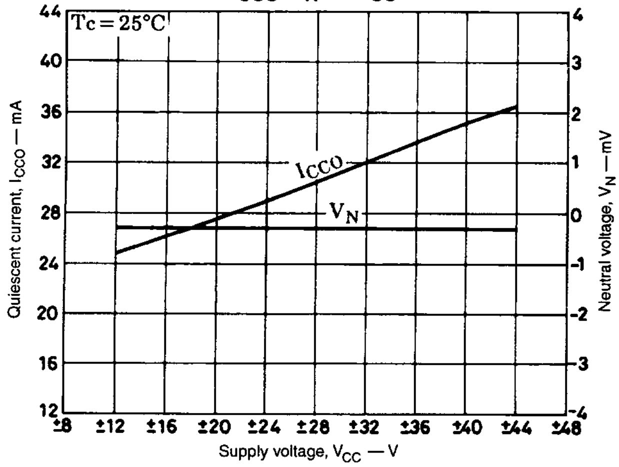


Test Circuit

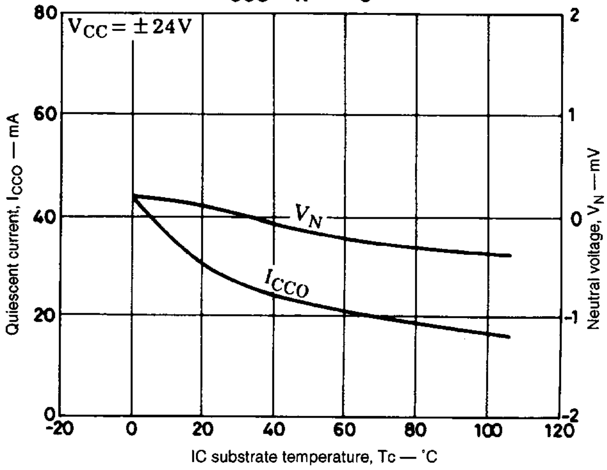


Vo : V_{NO} is measured by connecting a VTVM.
V_N is measured by connecting a DC voltmeter.
t_D is measured by connecting an oscilloscope.

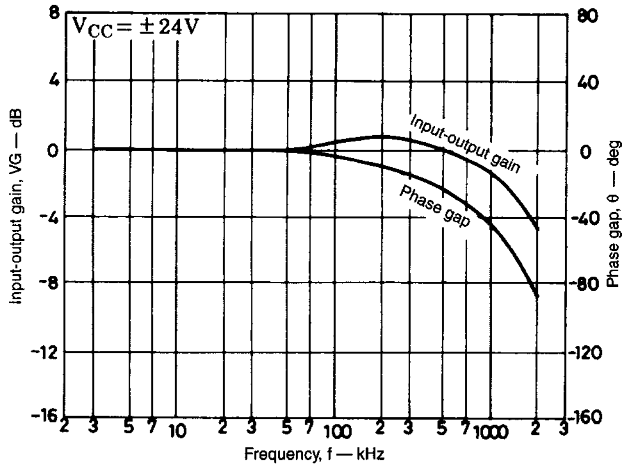
$I_{CCO}, V_N — V_{CC}$



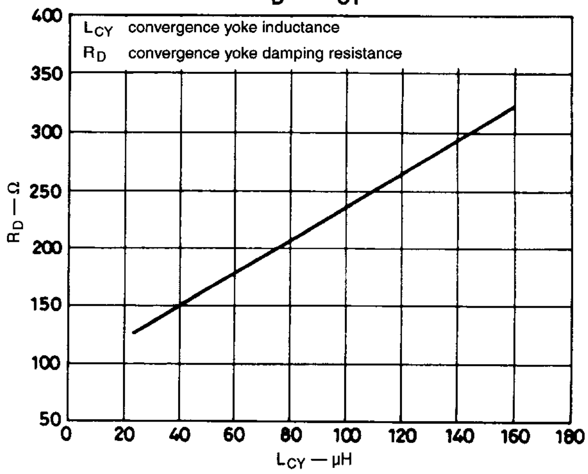
$I_{CCO}, V_N — T_C$



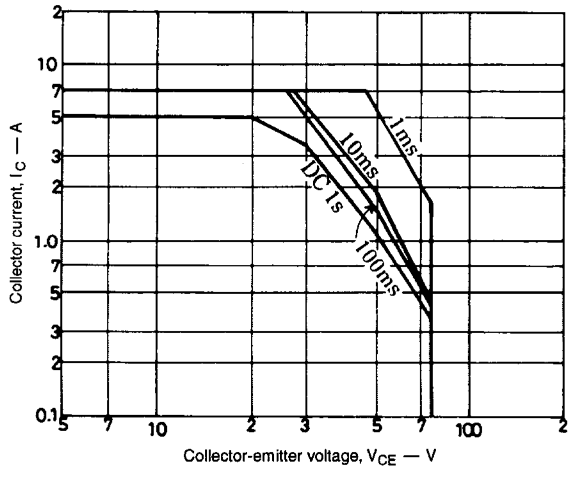
VG, θ — f



$R_D — L_{CY}$



Power transistor ASO



Maximum Ratings

Tj max, Tc max, θj-c

The heatsink design is determined by the maximum ratings of several key parameters–Tj max, Tc max and θj-c.

- Tj max (junction temperature)
  Tj max is dependent on the physical structure of each functional element. A junction temperature exceeding this rating can lead to device deterioration and breakdown, so the design must not exceed this rating.
- Tc max (operating substrate temperature)
  Tc max is dependent on the materials used within an element and on the circuit design, and should be selected on the basis of reliability. Operation exceeding this value is not guaranteed.
- θj-c (thermal resistance)
  θj-c is dependent on the heatsink design, which can vary greatly. the heatsink necessary is determined by calculation using the maximum rating for Tj.

As Tj and Tc operating conditions are independent, the heatsink must be designed to satisfy the maximum ratings for both parameters.

Heatsink Design Considerations

In the expressions below Pd represents the operating IC substrate internal power dissipation and Pc represents the power dissipation per transistor. The heatsink thermal resistance, θc-a, required to dissipate the total power dissipation, Pd, is determined as follows :

Condition 1: IC substrate temperature not to exceed 105°C

$$Pd \times \theta c\text{-}a + Ta < 105°C \text{ (Tc max)} \quad \ldots\ldots (1)$$

Where Ta is the guaranteed maximum ambient temperature.

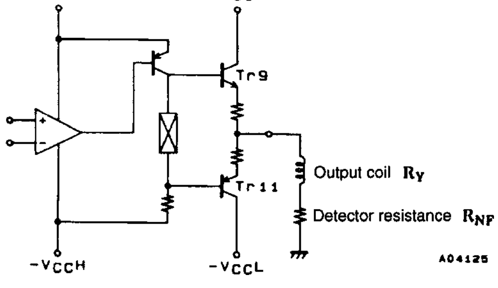
Condition 2: Power transistor junction temperature, Tj, not to exceed 150°C

$$Pd \times \theta c\text{-}a + Pc \times \theta j\text{-}c + Ta < 150°C \text{ (Tj max)} \quad \ldots\ldots (2)$$

Where θj-c is the power transistor thermal resistance per transistor. Therefore, the heatsink design must satisfy both these expression.

Design Process

A model circuit for a single channel in the STK319-020 is shown below.



The power dissipation, Pd, is the sum of channel 1, Pd1, and channel 2, Pd2, power dissipations.

$$Pd\ max = Pd1\ max + Pd2\ max$$

Therefore, form equation (1),

$$\theta c\text{-}a < \frac{Tc\ max - Ta\ max}{Pd\ max} \quad \ldots\ldots (3)$$

the necessary heatsink resistance is determined (note that Tc max=105°C)

The power dissipation per power transistor per channel, Pc, is related to the transistor junction temperature by the following equation.

$$Tj = Pd\ max \times \theta c\text{-}a + Ta + Pc \times \theta j\text{-}c \quad \ldots\ldots (4)$$

where Tj cannot exceed Tj max=105°C. Therfore, in order to maintain Tj below 150°C, a lower heatsink thermal resistance, θc-a, is necessary to lower Tc.

Heatsink Design Example

This example assumes the following worst-case conditions– $V_{CC}H=\pm35V$, $V_{CC}L=\pm25V$, output coil $L_Y=80\mu H$ and $R_Y=0\Omega$, current detector resistance $R_{NF}=4.7\Omega$, Ip-o max=0.6Ap-o (Ip-o (Ip-p=1.2A) sawtooth wave input, Io (DC) max=0.6A DC input, both chanels operating, Ta max=60°C (guaranteed maximum).

The channel1 power dissipation, Pd1, is given from Figures 1 and 2.

- Pd1 max=7.0W (AC) with sawtooth wave input
- Pd1 max=13.2W (DC) with DC input

As Pd1 max (AC) < Pd1 max (DC), the power dissipation is greater with DC input. Also, lokking at the output transistor dissipation, Pc,

- Pc=0.5Pd1 with sawtooth wave input
- Pc=Pd1 with DC input (one side transistor continuously ON)

the power dissipation is also higher with DC input. Accordingly, the heatsink design example below assumes DC input. The power dissipation in the predriver stage is ignored.

As Pd1 max=Pd2 max+13.2W, Pd max (both channels) is given by.

$$Pd\ max = Pd1\ max + Pd2\ max = 26.4W$$

From equation (3) with Ta=60°C,

$$\theta c\text{-}a = \frac{Tc\ max - Ta}{Pd\ max} = \frac{105-60}{26.4} = \ldots\ldots 1.70°C/W$$

For a 2mm aluminum heatsink with no surface coating, the necessary surface area, S, is given from Figure 3.

$$S = 780cm^2 \text{ (28cm} \times \text{28cm)}$$

Also from equation (4), the output stage power transistor jucntion temperature is given by

$$T_j = P_d\ max \times \theta c\text{-}a + T_a + P_c\ max \times \theta j\text{-}c$$
$$= 26.4 \times 1.7 + 60 + 13.2 \times 2.7$$
$$= 140.5°C$$

which provides a 9.5°C derating below Tj max=150°C. However, an allowance for the predriver stage power dissipation (transistors, resistors, etc.) should also be included in the substrate internal power dissipation, Pd.

Figure 1. Pd — Ip-o

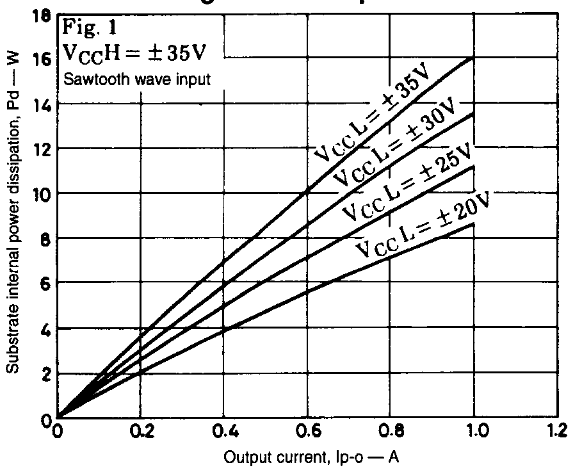


Figure 2. Pd — Io

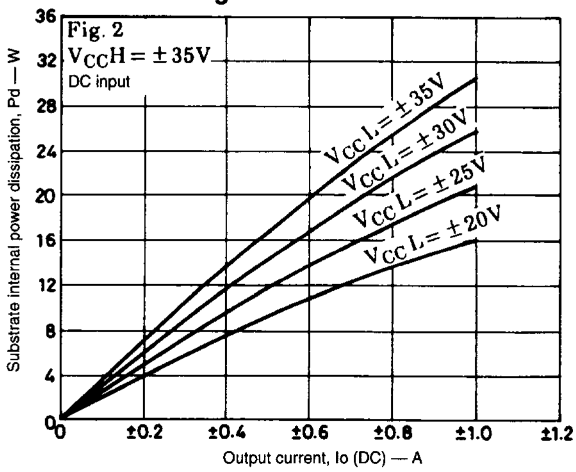
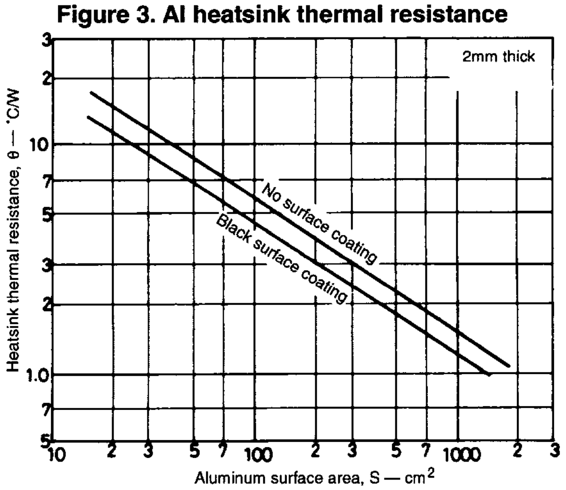


Figure 3. Al heatsink thermal resistance



This catalog provides information as of September, 1999. Specifications and information herein are subject to change without notice.