



DESCRIPTION

PT2315 is a two-channel digital audio processor utilizing CMOS Technology. Volume, Bass, Treble and Balance Controls are incorporated into a single chip. Loudness Function is also provided to build a highly effective electronic audio processor having the highest performance and reliability with the least external components. All functions are programmable using the I²C Bus. The pin assignments and application circuit are optimized for easy PCB layout and cost saving advantage for audio application. Housed in a 20-pin DIP/SOP, PT2315 is pin-to-pin compatible with TDA7315 and is very similar in performance with the later.

FEATURES

- CMOS technology
- Least external components
- Treble and Bass control
- Loudness function
- Input/output for external noise reduction system/equalizer
- 2 independent speaker controls for Balance function
- Independent mute function
- Volume control in 1.25dB/step
- Low distortion
- Low noise and DC stepping
- Controlled by I²C bus micro-processor interface
- Pin-to-pin compatible with TDA7315

APPLICATIONS

- Car stereo (Audio)
- Hi-Fi audio system
- Can be used in all I²C system applications

Note:

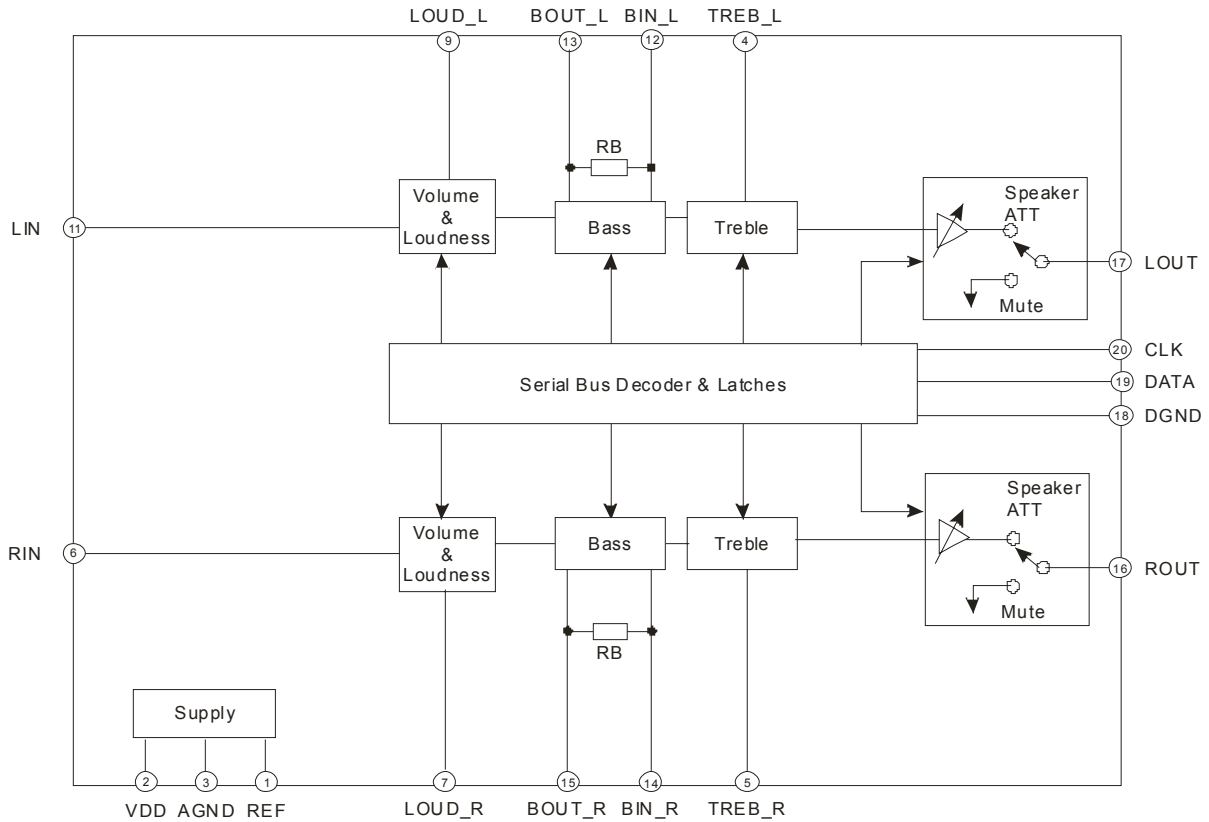
Purchase of I²C Component of Princeton Technology Corporation (PTC) conveys a license under Philips I²C Patent Right to use these components in any I²C System, provided that the system conforms to the I²C Standard Specification defined by Philips



2-Channel Audio Processor IC

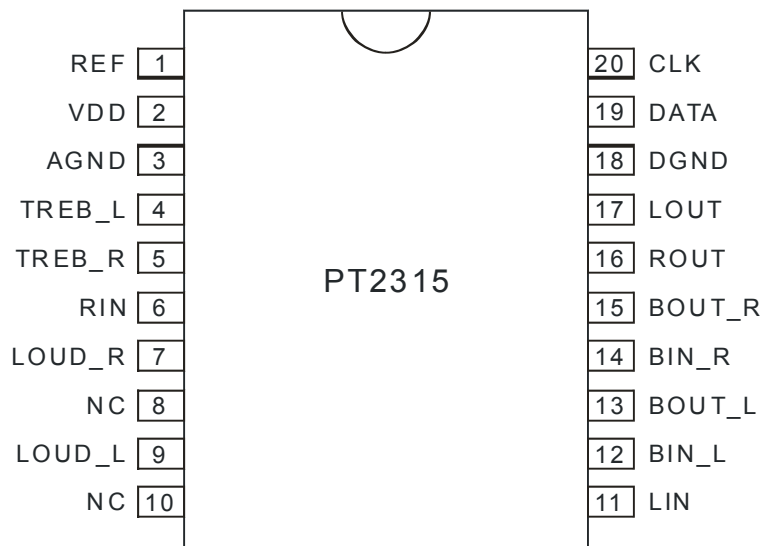
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BLOCK DIAGRAM





PIN CONFIGURATION





PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
REF	-	Analog Reference Voltage (1/2 VDD)	1
VDD	-	Supply Input Voltage	2
AGND	-	Analog Ground	3
TREB_L	I	Left Channel Input for Treble Controller	4
TREB_R	I	Right Channel Input for Treble Controller	5
RIN	I	Audio Processor Right Channel Input	6
LOUD_R	I	Right Channel Loudness Input	7
LOUD_L	I	Left Channel Loudness Input	9
LIN	I	Audio Processor Left Channel Input	11
BIN_L	I	Left Bass Controller Input Channel	12
BOUT_L	O	Left Bass Controller Output Channel	13
BIN_R	I	Right Bass Controller Input Channel	14
BOUT_R	O	Right Bass Controller Output Channel	15
ROUT	O	Right Speaker Output	16
LOUT	O	Left Speaker Output	17
DGND	-	Digital Ground	18
DATA	I	Control Data Input	19
CLK	I	Clock Input for Serial Data Transmission	20
NC	-	No Connection	8, 10



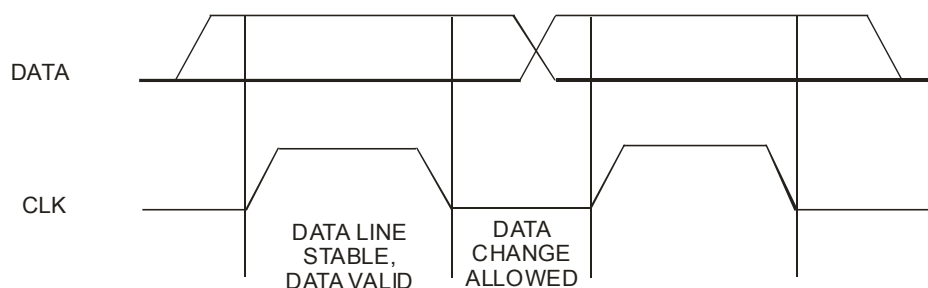
FUNCTION DESCRIPTION

I²C BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2315 via the DATA and CLK. The DATA and CLK make up the BUS Interface.

DATA VALIDITY

A data on the DATA Line is considered valid and stable only when the CLK Signal is in HIGH State. The HIGH and LOW State of the DATA Line can only change when the CLK signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

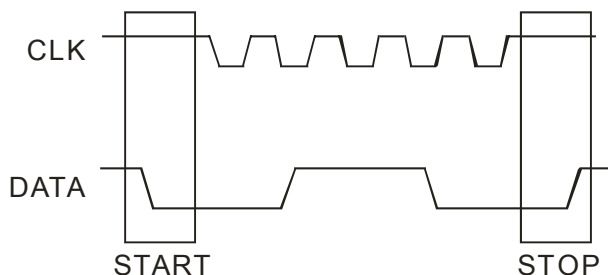
A Start Condition is activated when

1. CLK is set to HIGH and
2. DATA shifts from HIGH to LOW State.

The Stop Condition is activated when

1. CLK is set to HIGH and
2. DATA shifts from LOW to HIGH State

Please refer to the timing diagram below.





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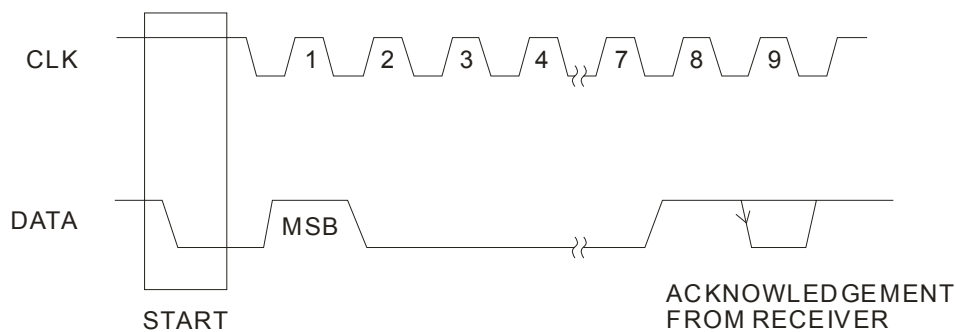
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BYTE FORMAT

Every byte transmitted to the DATA Line consist of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μ P) puts a resistive HIGH level on the DATA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the DATA line during the Acknowledge Clock Pulse so that the DATA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an acknowledge after receiving each byte, otherwise, the DATA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

TRANSMISSION WITHOUT ACKNOWLEDGE

If you want to avoid the acknowledge detection of the audio processor, a simpler μ P transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.



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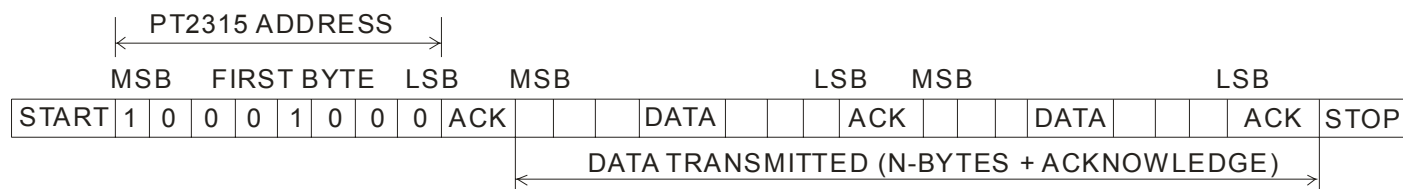
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INTERFACE PROTOCOL

The interface protocol consists of the following:

- A Start Condition
- A Chip Address Byte including the PT2315 address. The 8th Bit of the Byte must be "0". PT2315 must always acknowledge the end of each transmitted byte.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition

Please refer to the diagram below:



Notes:

1. ACK=Acknowledge
2. Max. Clock Speed=100Bits/s



2-Channel Audio Processor IC

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SOFTWARE SPECIFICATION

PT2315 ADDRESS

PT2315 Address is shown below.

1 MSB	0	0	0	0	0	0	0	0 LSB
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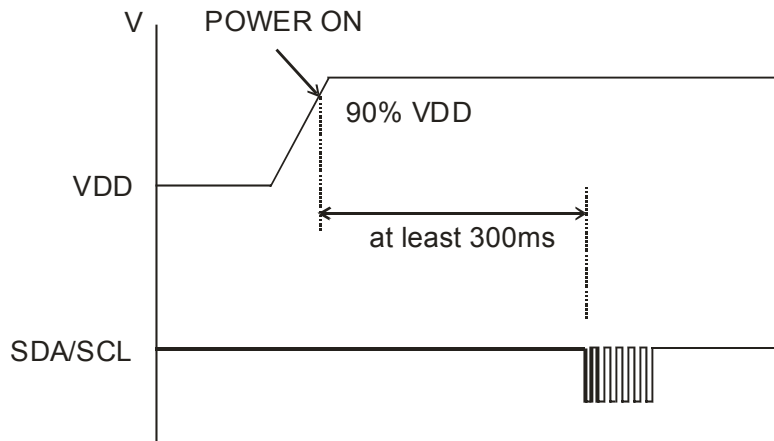
DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Speaker ATT L
1	0	1	B1	B0	A2	A1	A0	Speaker ATT R
0	1	0	*	*	L	*	*	Loudness Control
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

where Ax=1.25 dB steps; Bx=10 dB steps; Cx=2 dB steps; * =no effect

I²C BUS INTERFACE START TIME

After Power is turned ON, PT2315 needs to wait for a short time in order to insure stability. This waiting period is relative to the value of Cref. As the Cref value is 10µf, the waiting time period for PT2315 to send I²C Bus Signal is at least 300ms. If the waiting time period is less than 300ms, I²C Control may fail. Please refer to the diagram below.





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VOLUME

The table below gives a detailed description of the Volume Data Bytes. For example, a volume of -37.5 dB is given by 0 0 0 1 1 1 1 0.

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

SPEAKER ATTENUATORS

The table below gives a detailed description of the speaker attenuators data bytes. For example, an attenuation of 30dB on the Speaker L (Left) is given by 1 0 0 1 1 0 0 0.

MSB							LSB	Function
1	0	0	B1	B0	A2	A1	A0	Speaker L
1	0	1	B1	B0	A2	A1	A0	Speaker R
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute



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LOUDNESS FUNCTION

The following table shows the detailed description of the Loudness Function. For example, when the Loudness Function is turned ON, the code format is 0 1 0 0 0 0 0.

MSB							LSB	Function
0	1	0	*	*	L	*	*	Loudness Control
					0			Loudness ON
					1			Loudness OFF

Note: *=No Effect

BASS AND TREBLE DATA BYTES

The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at -12dB is given by 0 1 1 1 0 0 1.

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Operating supply voltage	V _s		10.5	V
Input current, any pin except supplies	I _{in}	-10	10	mA
Input voltage (see Note)	V _{in}	-0.3	V _S +0.3	V
Operating temperature	T _{opr}	-40	85	°C
Storage temperature	T _{stg}	-65	150	°C

QUICK REFERENCE DATA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _S	6	9	10	V
Max. input signal handling	V _{CL}	2	2.5	-	V _{rms}
Total harmonic distortion (V=1V _{rms} , f=1KHz)	THD	-	0.07	0.15	%
Signal to noise ratio	S/N	-	95	-	dB
Channel separation (f=1KHz)	Sc	-	85	-	dB
Volume control 1.25dB step	-	-75	-	0	dB
Bass & Treble control 2dB step	-	-14	-	+14	dB
Balance control 1.25dB step	-	-37.5	-	0	dB
Mute attenuation	-	-	75	-	dB



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ELECTRICAL CHARACTERISTICS

(Unless specified: $T_a=25^{\circ}\text{C}$, $V_{DD}=9\text{V}$, $R_L=100\text{K}\Omega$, $R_g=600\Omega$, all controls flat$G=0$, $f=1\text{KHz}$)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply						
Supply voltage	V_{DD}		6	9	10	V
Supply current	I_S		-	30	40	mA
Volume Control						
Input resistance	R_{IV}		20	30	40	$\text{K}\Omega$
Control range	C_{RANGE}		65	70	75	dB
Min. attenuation	$A_{V_{MIN}}$		-1	0	1	dB
Max. attenuation	$A_{V_{MAX}}$		65	70	75	dB
Step resolution	A_{STEP}		0.5	1.25	1.75	dB
Attenuation set error	E_A	$A_V=0$ to -20dB	-1.25	0	1.25	dB
		$A_V=-20$ to -60dB	-3.0		2	dB
Speaker Attenuators						
Control range	C_{RANGE}		35	37.5	40	dB
Step resolution	S_{STEP}		0.5	1.25	1.75	dB
Attenuation set error	E_A		-	-	1.5	dB
Output mute attenuation	A_{MUTE}		70	75	-	dB
Bass Control (see Note)						
Control range	G_b	Max. Boost/Cut	± 12	± 14	± 16	dB
Step resolution	B_{STEP}		1	2	3	dB
Internal feedback resistance	R_B		34	44	58	$\text{K}\Omega$
Treble Control (see Note)						
Control range	G_t	Max. Boost/Cut	± 13	± 14	± 15	dB
Step resolution	T_{STEP}		1	2	3	dB
Audio Outputs						
Clipping level	V_{OCL}	$A_V=-8.75\text{dB}$, $d=0.3\%$	2	2.5	-	V _{rms}
Output resistance	R_{OUT}		-	40	45	Ω
DC voltage level	V_{OUT}		4.2	4.5	4.8	V



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Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
General						
Output noise	N _O	BW=20~20KHz, Flat output muted All gains=0dB	-	-97 -92	-	dB dB
		A Curve All Gains=0dB	-	-100	-	dB
Signal to noise ratio	S/N	All Gains=0dB V _O =1Vrms	-	95	-	dB
Distortion	d	A _V =0, V _{IN} =1Vrms	-	0.1	0.3	%
		A _V =-8.75dB, V _{IN} =1Vrms	-	0.07	0.15	%
		A _V =-8.75dB, V _{IN} =0.3Vrms	-	0.03	0.1	%
Channel separation left/right	Sc		80	90	-	dB
Bus Inputs						
Input low voltage	V _{IL}		-	-	1	V
Input high voltage	V _{IH}		3	-	-	V
Input current	I _{IN}		-5	-	+5	μA
Output voltage SDA acknowledge	V _O	I _O =1.6mA	-	-	0.4	V

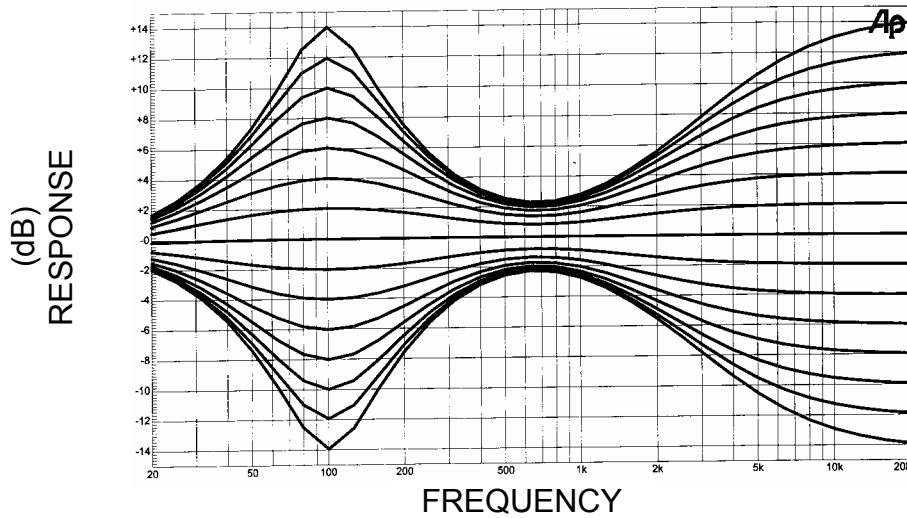
Note:

For the Bass and Treble Response, please refer to the diagram below. The center frequency and quality of the resonance behavior can be selected by the external circuitry. A standard first order bass response can realized by a standard feedback network.

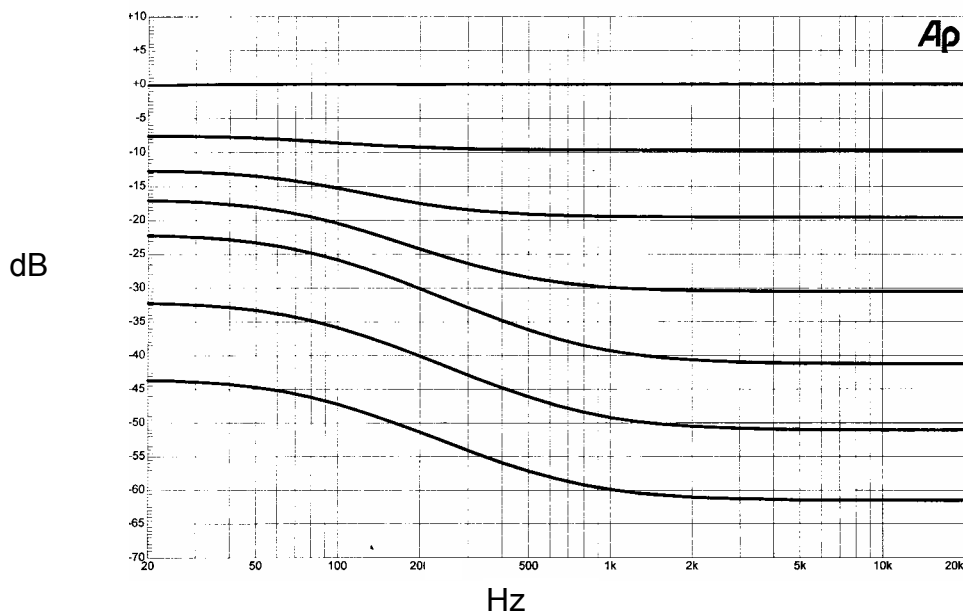


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Typical Tone Response (with the ext. Components indicated in the test circuit)

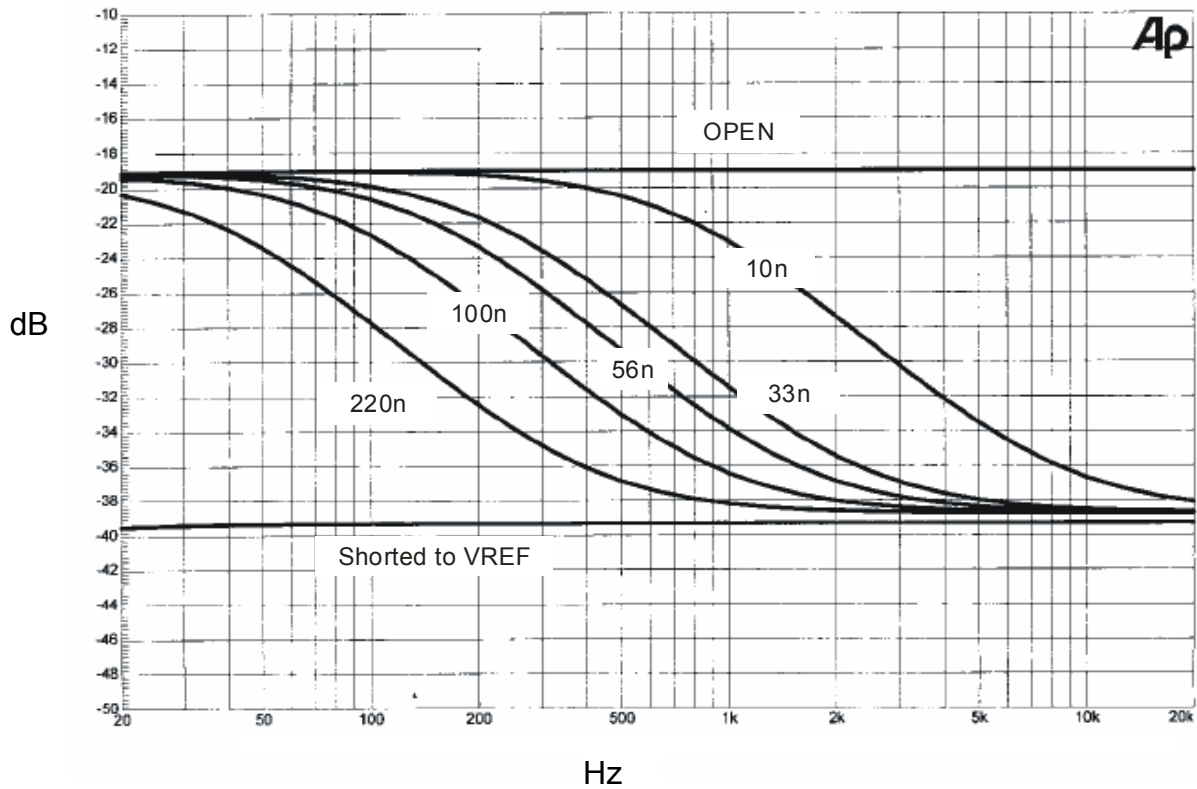


Loudness vs Volume Attenuation Frequency Response ($C_{10}=C_{11}=100\text{nF}$)



2-Channel Audio Processor IC

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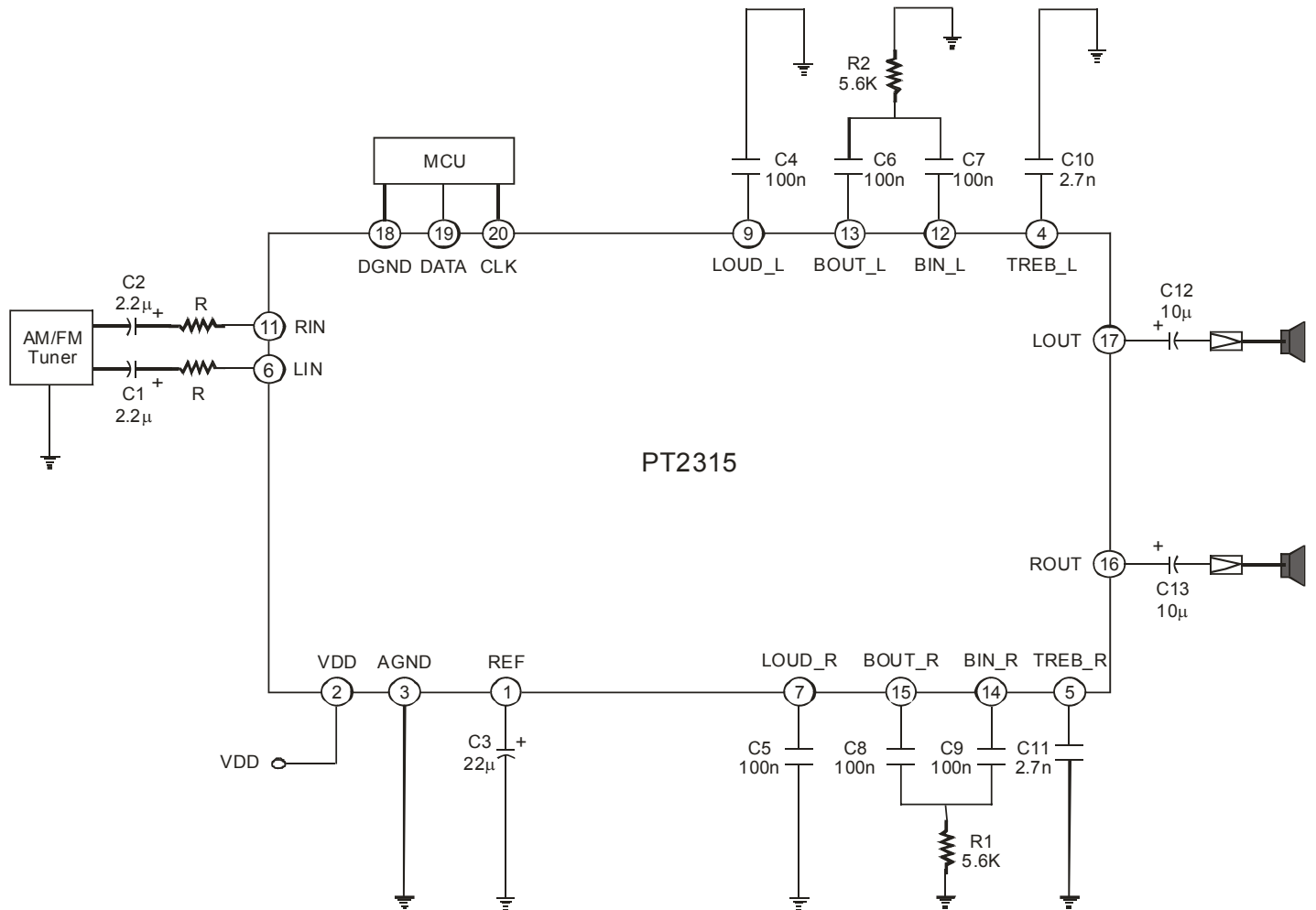
C₁₀, C₁₁ vs Loudness Frequency Response (Volume=-40dB, All other controls are flat)



2-Channel Audio Processor IC

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APPLICATION CIRCUIT



Notes:

1. The Resistor (R) range=2.0KΩ ~ 3.6KΩ.
2. Resistor (R) Recommended Value=2.4KΩ.



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2315	20 Pins, SOP, 300mil	PT2315
PT1215-D	20 Pins, DIP, 300mil	PT2315-D
PT2315 (L)	20 Pins, SOP, 300mil	PT2315
PT2315-D (L)	20 Pins, DIP, 300mil	PT2315-D

Notes:

1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the data code.

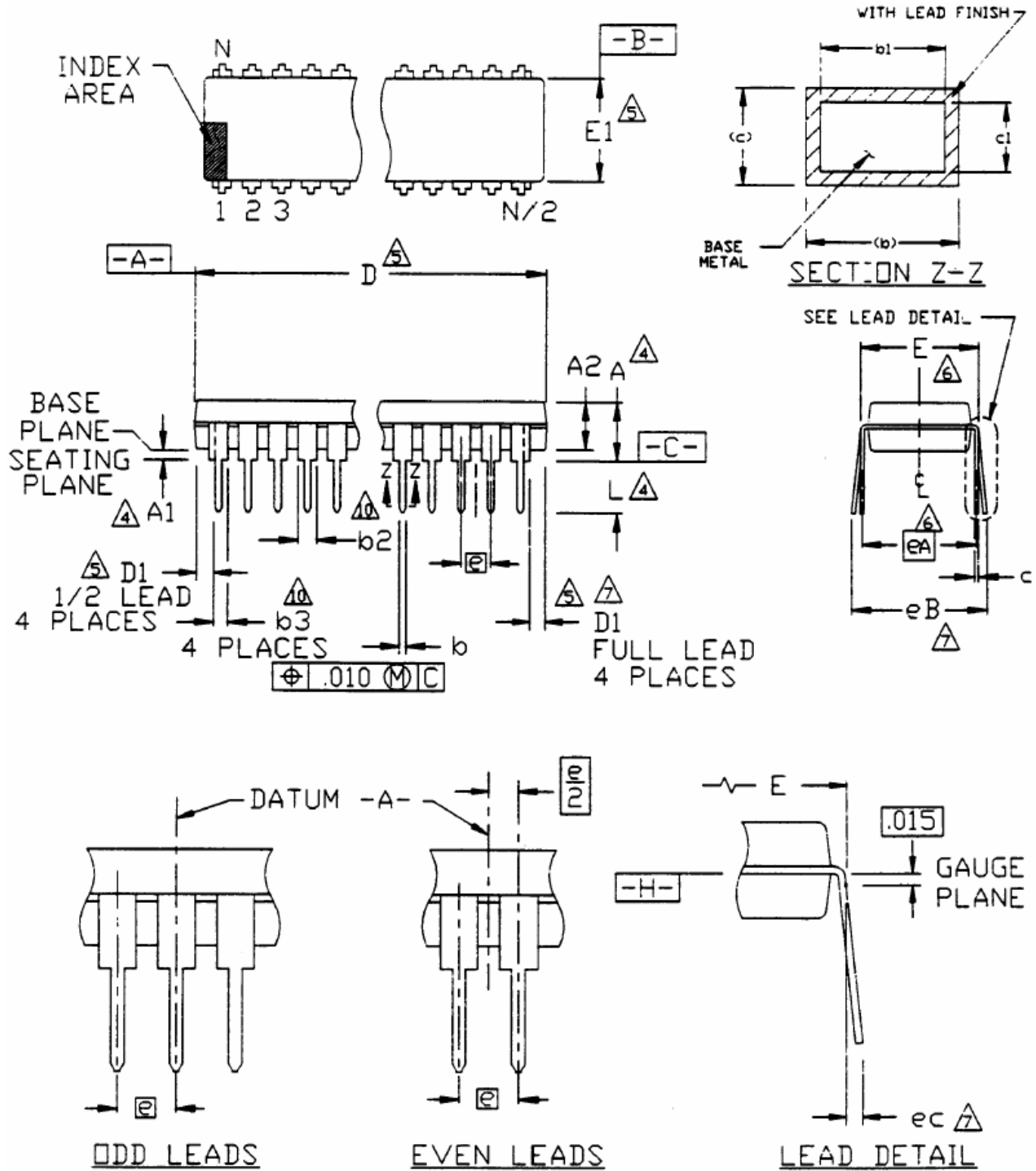


2-Channel Audio Processor IC

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PACKAGE INFORMATION

20 PINS, DIP, 300 MIL





2-Channel Audio Processor IC

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Symbol	Dimensions In Inches		
	Min.	Nom.	Max.
A			0.210
A1	0.015		
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.980	1.030	1.060
D1	0.005		
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 bsc.		
eA	0.300 bsc.		
eB			0.430
eC	0.000		0.060
L	0.115	0.130	0.150

Notes:

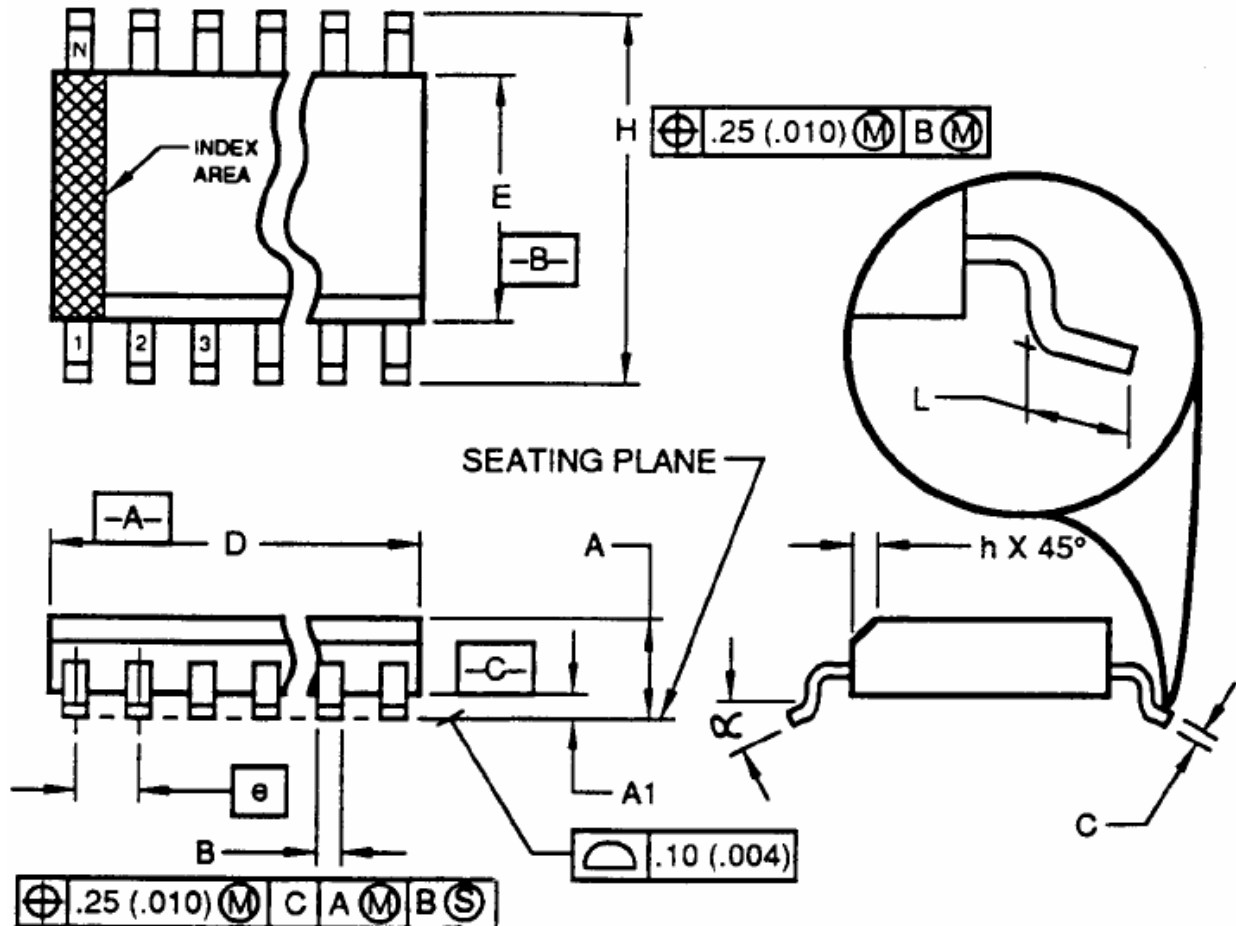
- All dimensions are in INCHES.
 - Dimensioning and tolerancing per ANSI Y14.5M-1982.
 - Dimension "A", "A1" and "L" are measured with the package seated in JEDEC Seating Plane Gauge GS-3
 - "D", "D1" and "E1" dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
 - "E" and "eA" measured with the leads constrained to be perpendicular to datum $\square\text{-C-}$.
 - "eB" and "eC" are measured at the lead tips with the leads unconstrained.
 - N is the number of the terminal positions (N=20)
 - Pointed or rounded lead tips are preferred to ease insertion.
 - "b2" and "b3" maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm)
 - Distance between leads including Dambar protrusions to be 0.005 inch minimum.
 - Datum plane $\square\text{-H-}$ coincident with the bottom of lead, where lead exits body.
 - Refer to JEDEC MS-001, Variation AD.
- JEDEC is the trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.



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20 PINS, SOP, 300MIL



Symbol	Dimensions In Millimeter		
	Min.	Nom.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	12.60		13.00
E	7.40		7.60
e		1.27 bsc.	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
α	0°		8°



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Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
 3. Dimension "E" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm (0.010 in) per side.
 4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
 5. "L" is the length of the terminal for soldering to a substrate.
 6. N is the number of the terminal positions (N=20)
 7. The lead width "B" as measured 0.36mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.24 in).
 8. Controlling dimension: MILLIMETER.
 9. Refer to JEDEC MS-013, Variation AC.
- JEDEC is the trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.