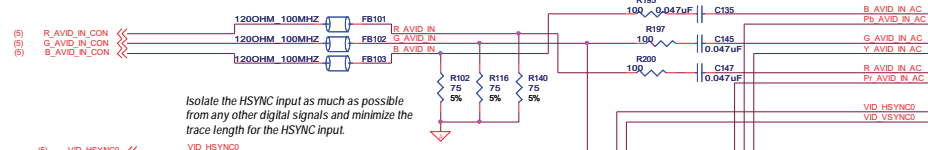


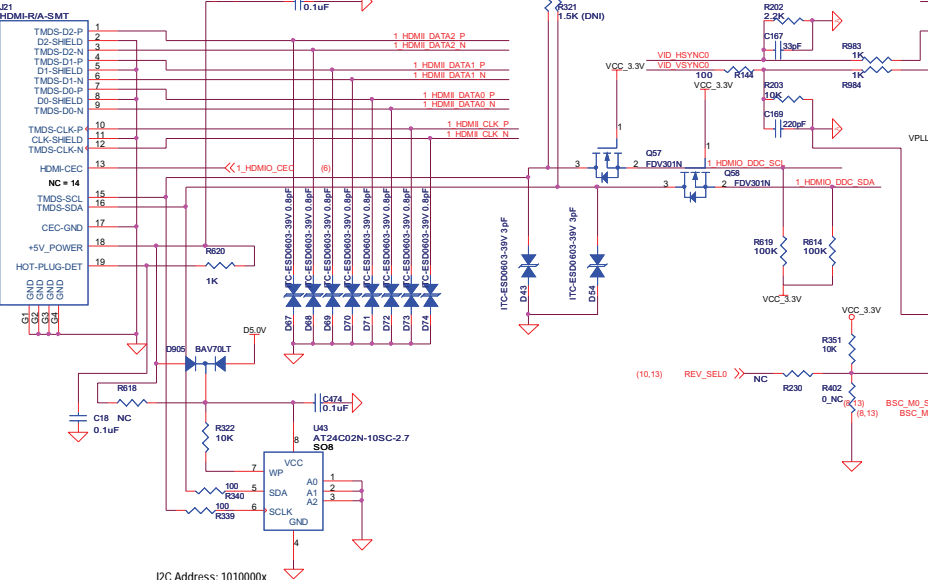
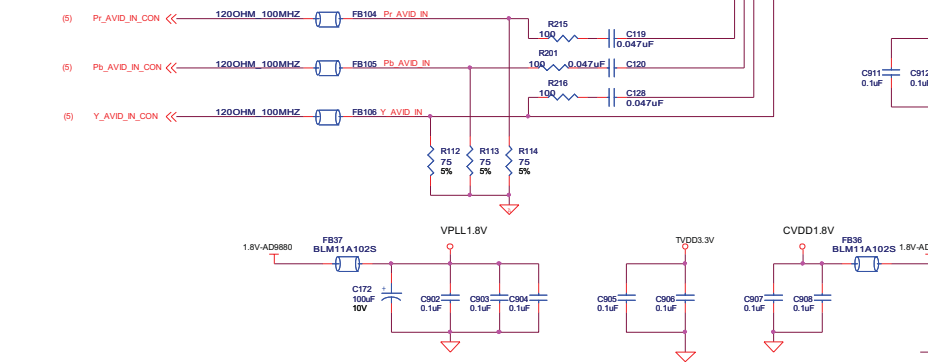
Use 75 ohm matched impedance traces.



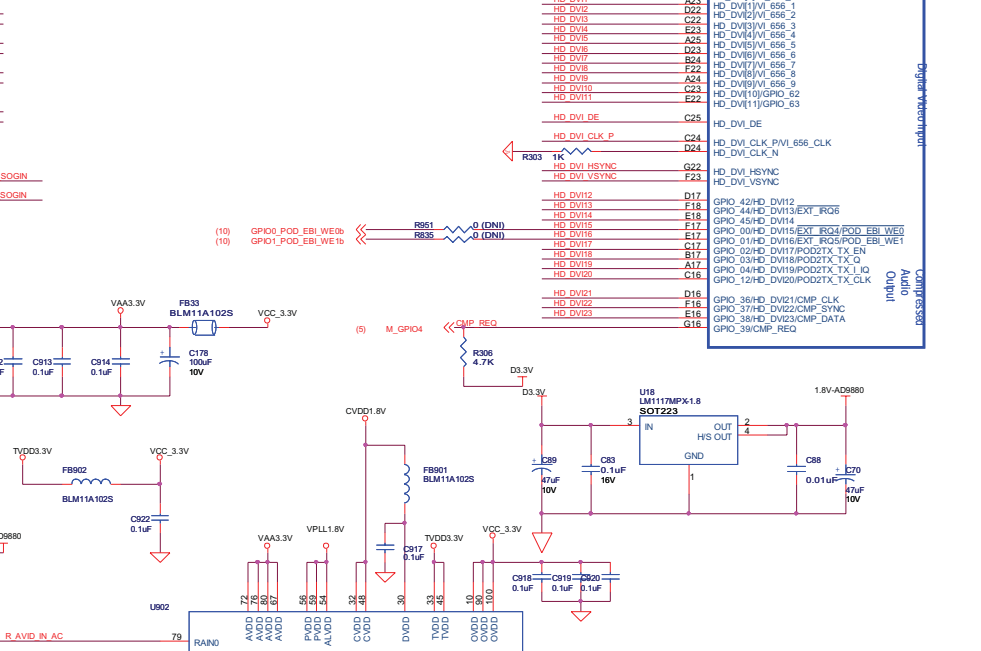
Isolate the HSYNC input as much as possible from any other digital signals and minimize the trace length for the HSYNC input.

Minimize the trace length running into the graphics input. This is accomplished by placing the 3586 as close as possible to the graphics VGA connector.

Place the 75 ohm termination resistors as close as possible to the 9880chip.

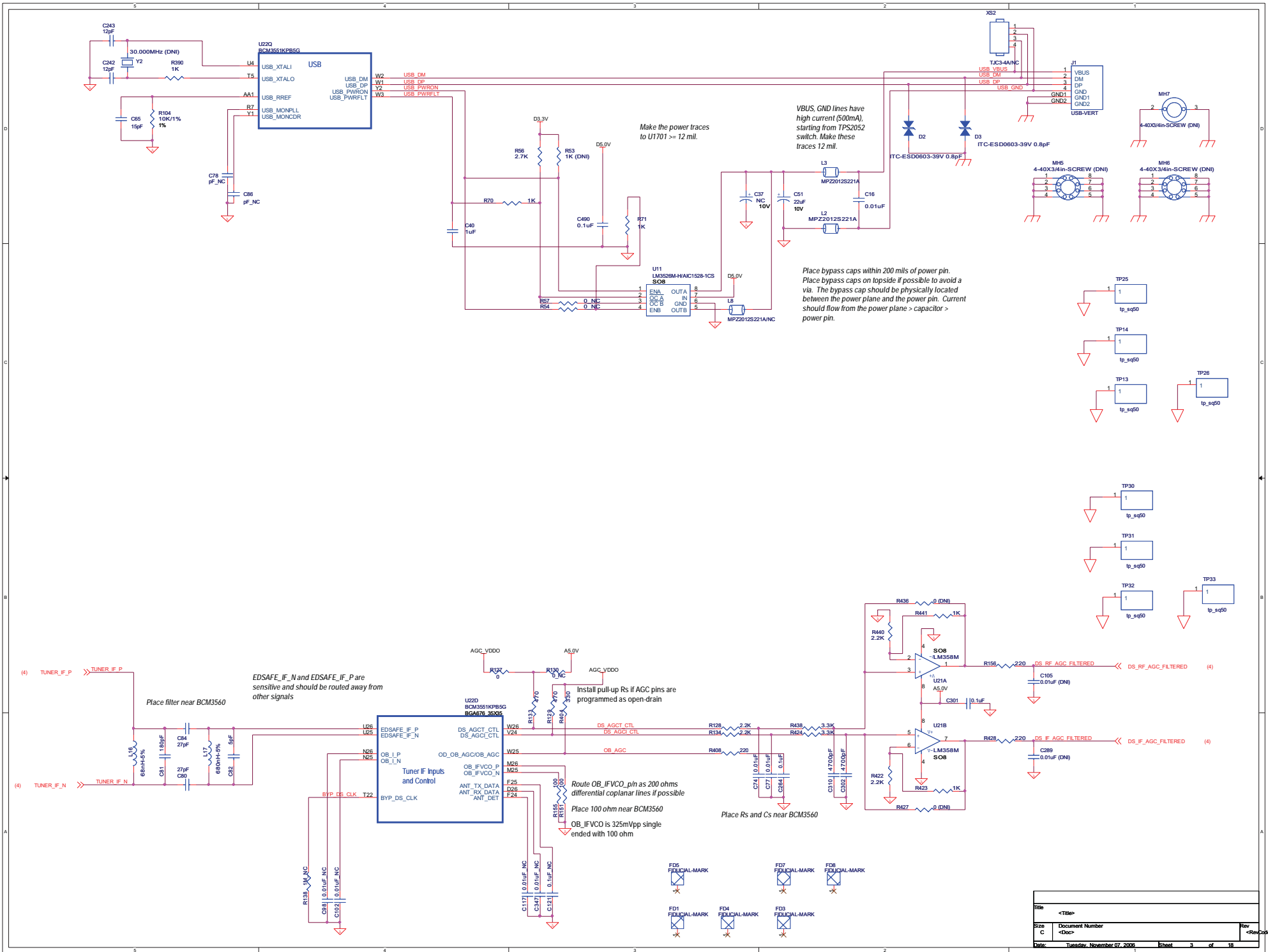


I2C Address: 1010000x



AD9880KSTZ-100

Pin	Signal	Notes
R23	HD_DV[0]/VI_656_0	
A23	HD_DV[1]/VI_656_1	
D22	HD_DV[2]/VI_656_2	
C22	HD_DV[3]/VI_656_3	
E23	HD_DV[4]/VI_656_4	
A25	HD_DV[5]/VI_656_5	
D23	HD_DV[6]/VI_656_6	
B24	HD_DV[7]/VI_656_7	
F24	HD_DV[8]/VI_656_8	
A24	HD_DV[9]/VI_656_9	
C23	HD_DV[10]/GPIO_B2	
E22	HD_DV[11]/GPIO_B3	
C25	HD_DVI_DE	
D24	HD_DVI_CLK_P	
D24	HD_DVI_CLK_N	
G22	HD_DVI_HSYNC	
F23	HD_DVI_VSYNC	
D17	GPIO_42/HD_DV[12]	
F18	GPIO_44/HD_DV[13]/EXT_IRQ3	
E18	GPIO_45/HD_DV[14]	
F17	GPIO_00/HD_DV[15]/EXT_IRQ4/POD_EBI_WE0	
E17	GPIO_01/HD_DV[16]/EXT_IRQ5/POD_EBI_WE1	
C17	GPIO_02/HD_DV[17]/POD2TX_TX_EN	
B17	GPIO_03/HD_DV[18]/POD2TX_TX_Q	
A17	GPIO_04/HD_DV[19]/POD2TX_TX_I_Q	
D16	GPIO_12/HD_DV[20]/POD2TX_TX_CLK	
C16	GPIO_36/HD_DV[21]/CMP_CLK	
F16	GPIO_37/HD_DV[22]/CMP_SYNC	
E16	GPIO_38/HD_DV[23]/CMP_DATA	
G16	GPIO_39/CMP_REQ	



Make the power traces to U1701 >= 12 mil.

VBUS, GND lines have high current (500mA), starting from TPS2052 switch. Make these traces 12 mil.

Place bypass caps within 200 mils of power pin. Place bypass caps on topside if possible to avoid a via. The bypass cap should be physically located between the power plane and the power pin. Current should flow from the power plane > capacitor > power pin.

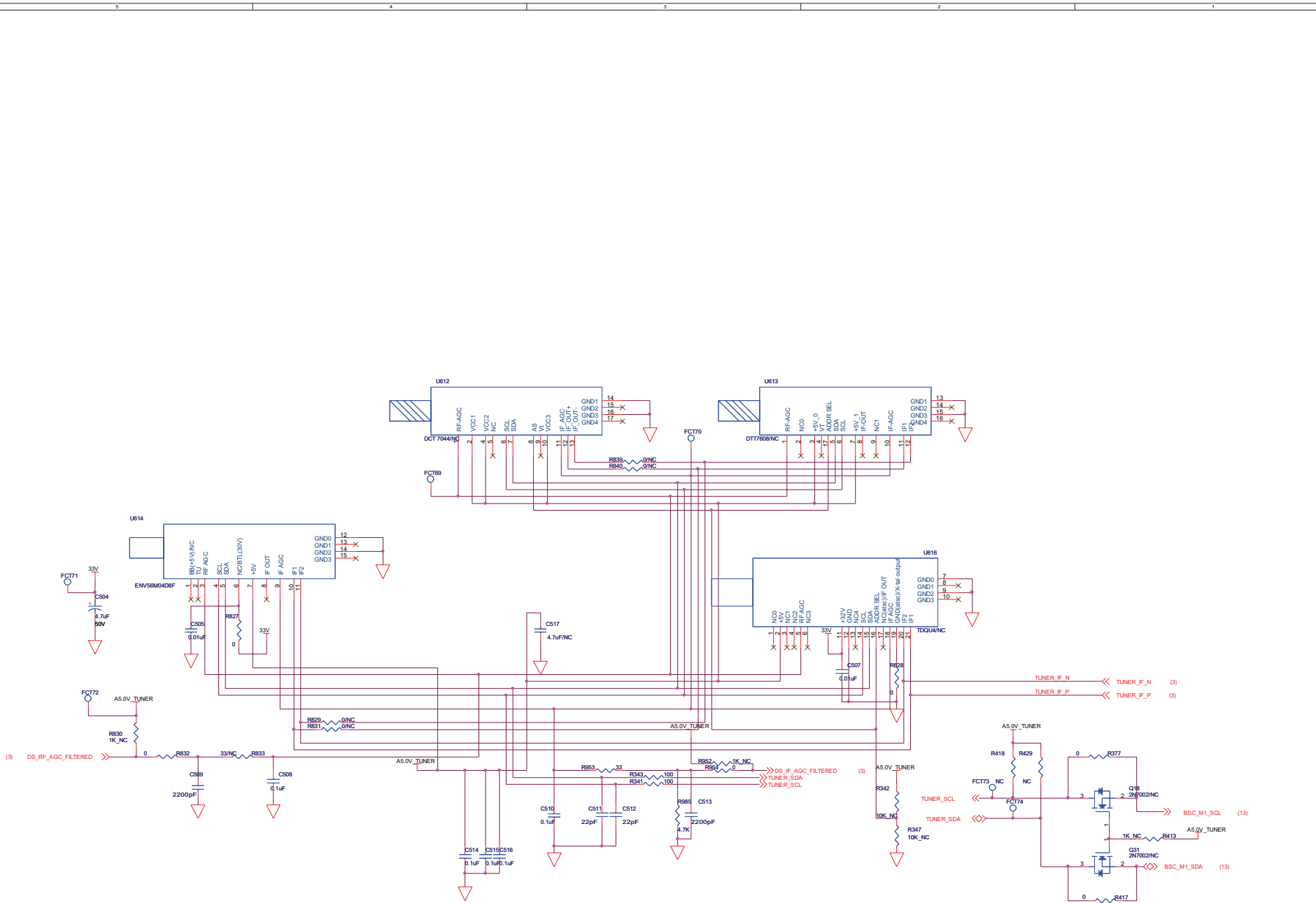
EDSAFE_IF_N and EDSAFE_IF_P are sensitive and should be routed away from other signals

Install pull-ups if AGC pins are programmed as open-drain

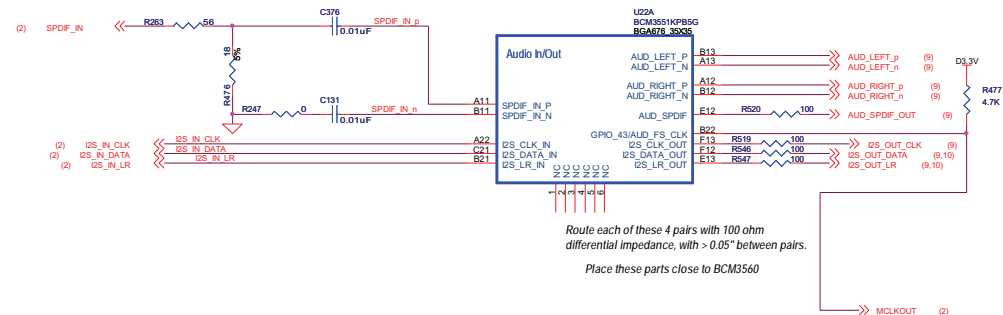
Route OB_IFVCO_p/h as 200 ohms differential coplanar lines if possible

Place 100 ohm near BCM3560
OB_IFVCO is 325mVpp single ended with 100 ohm

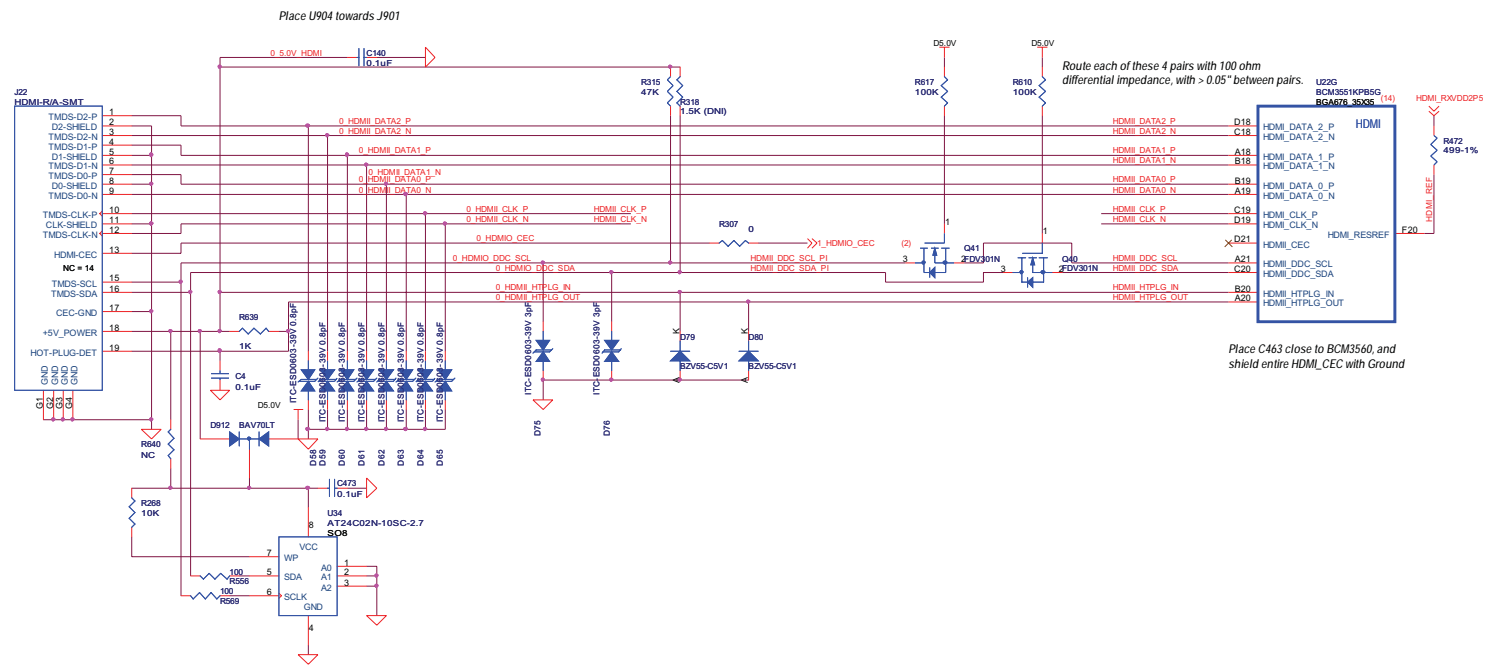
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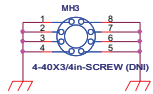
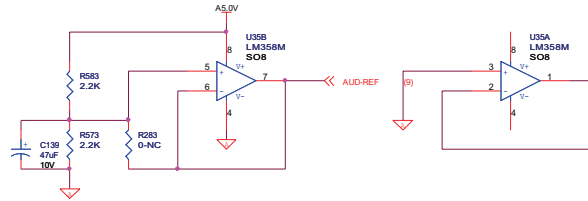
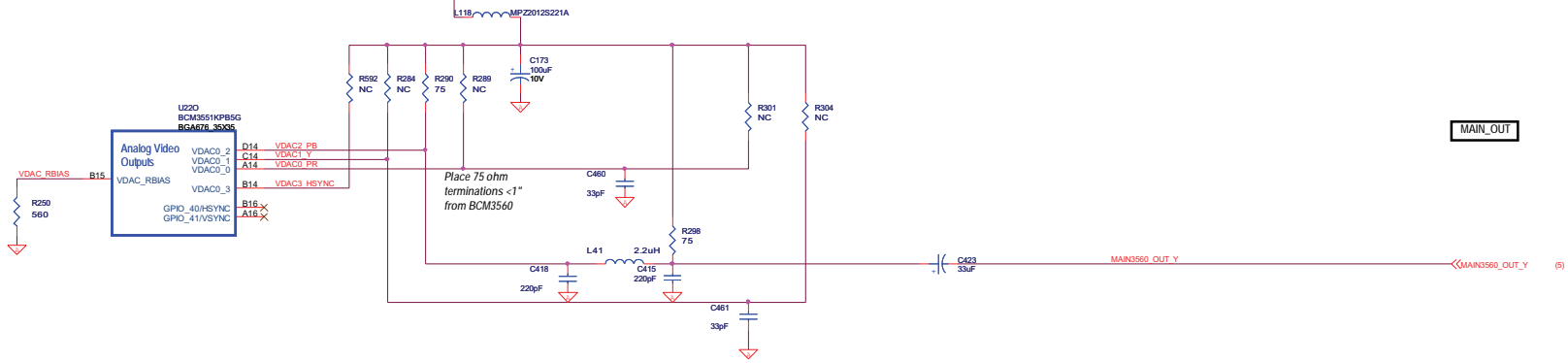
Route each of these 4 pairs with 100 ohm differential impedance, with > 0.05" between pairs.
Place these parts close to BCM3560



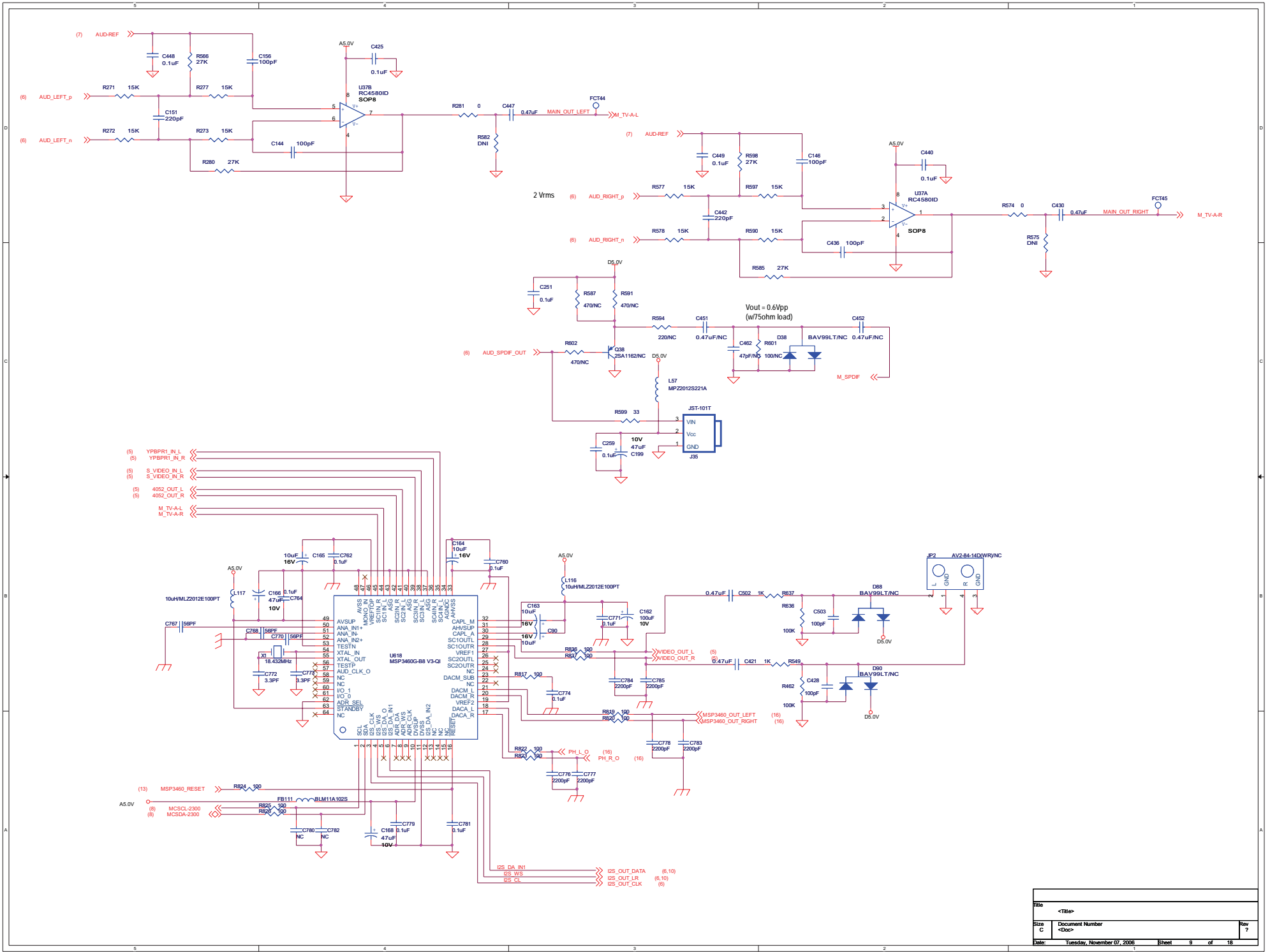
Place C463 close to BCM3560, and shield entire HDMI_CEC with Ground

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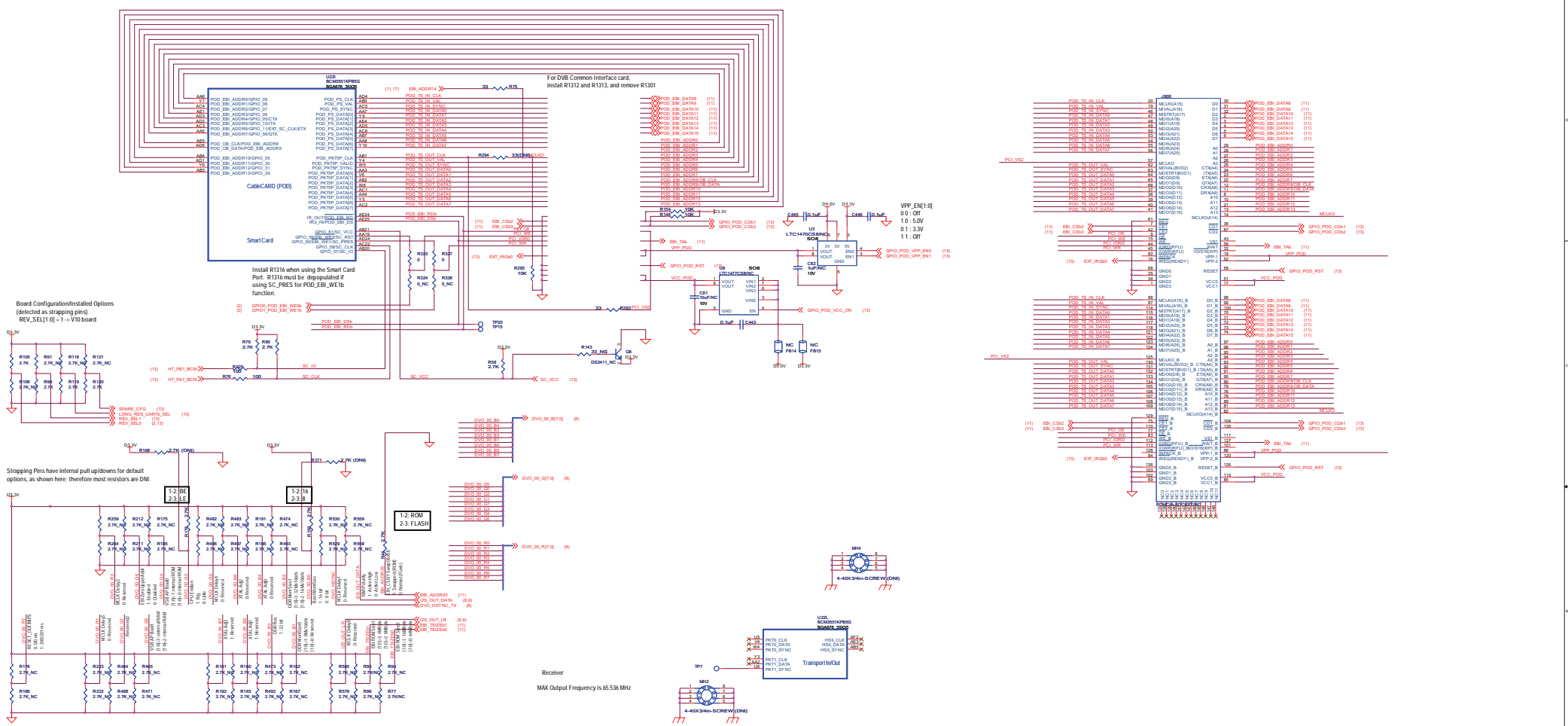
VDAC_AVDD33 needs to be very clean. If you use switching supplies, consider using a small linear regulator for this supply. (250 mA worst case)
 Route VDAC_AVDD33 as a wide trace or fill area on the top layer of the PCB all the way to the connector



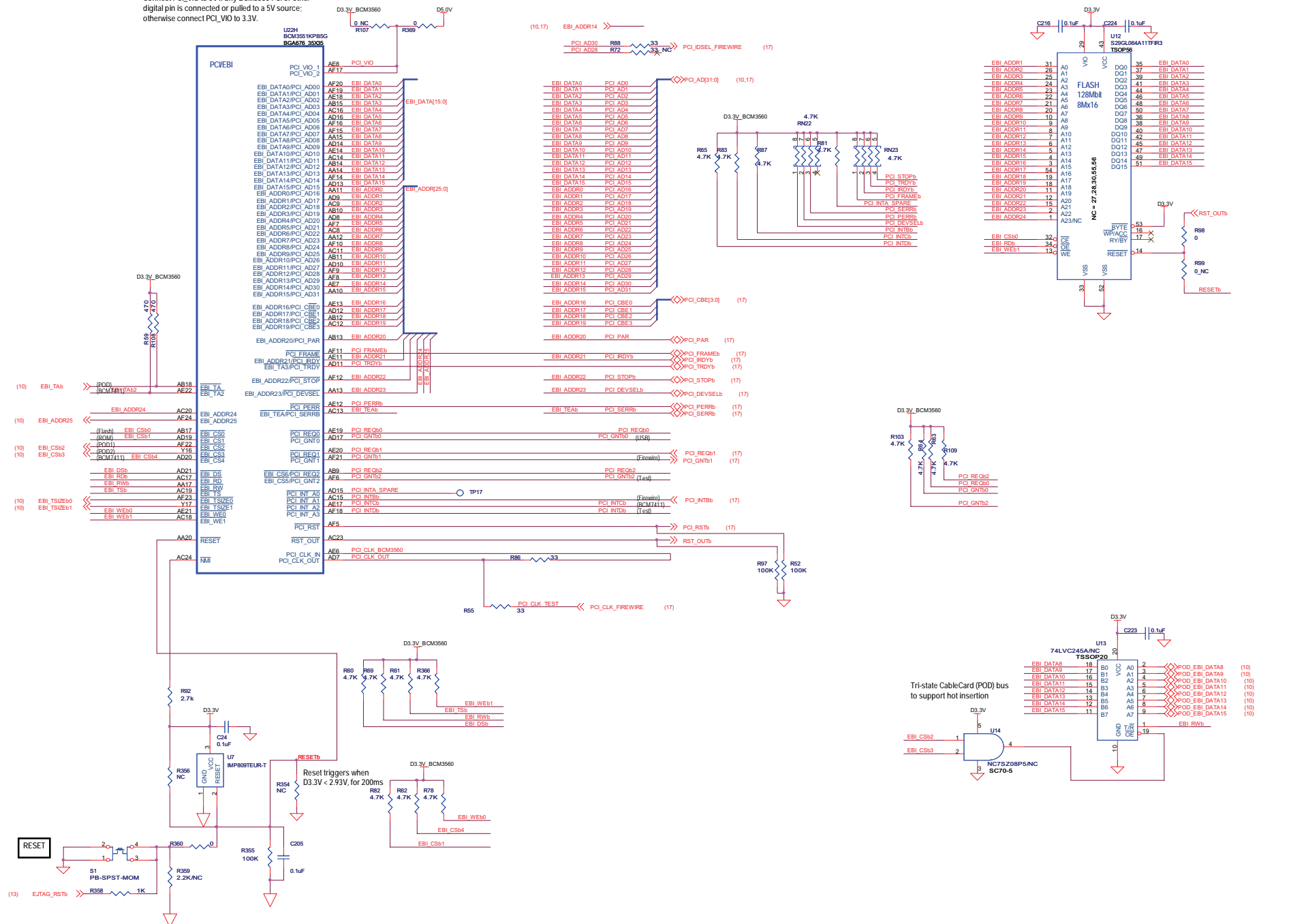
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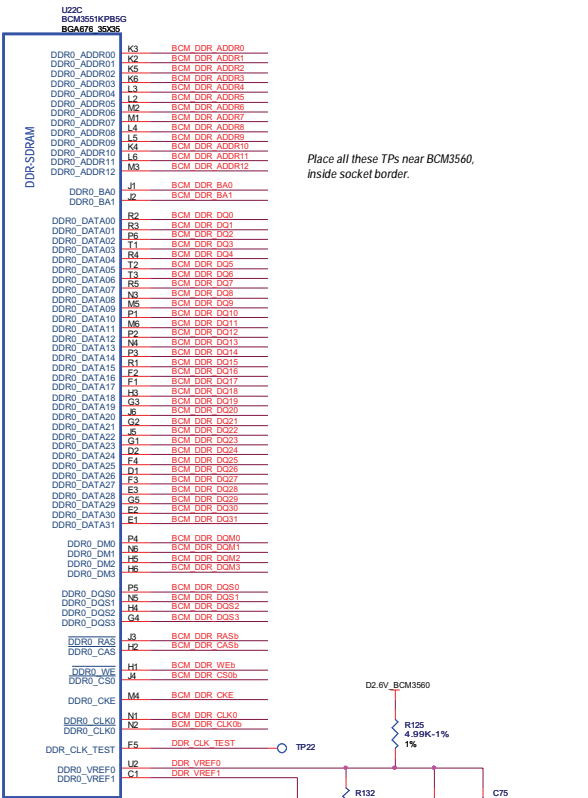


Connect PCI_VIO to 5V if any BCM3560 PCI or other digital pin is connected or pulled to a 5V source; otherwise connect PCI_VIO to 3.3V.

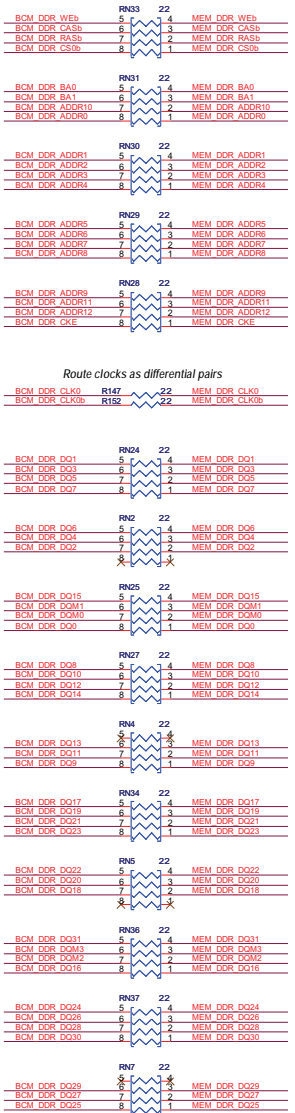


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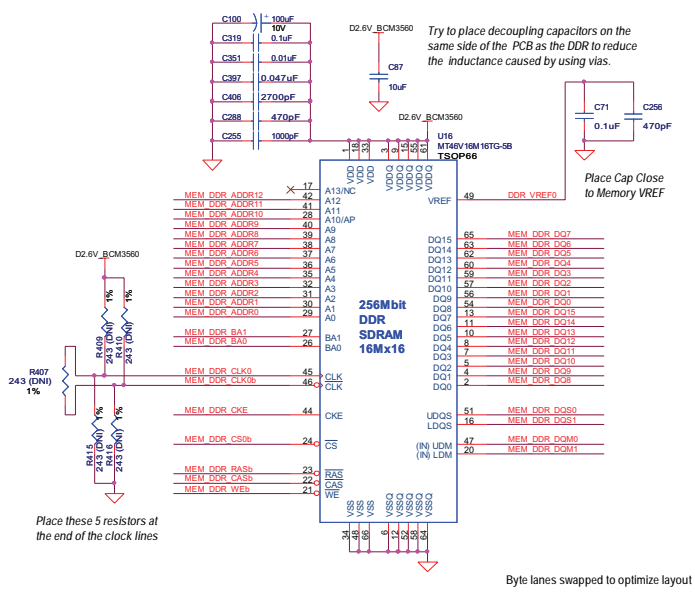
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Place all these TPs near BCM3560, inside socket border.



- New DDR routing rules:**
- All timing is relative to the CLK/CLKb that arrive at the destination DDR SDRAM chip.
- 1) $X = \text{CLK/CLKb}$ should be a matched differential pair with a length $< 4''$
 - 2) Address and control should be $X \pm 0.75''$ (or 100 ps)
 - 3) DQS and DOM should be $X \pm 0.75''$ (or 100 ps)
 - 4) All DOs should match corresponding byte lane DOS/DOMs within $\pm 0.20''$ (or 30 ps)
 - 5) Place 22 ohm resistors for DO and DQS bidirectional lines half-way between BCM and Memory.
 - 6) Place 22 ohm resistors for CLK, ADDR, BA, DM, RAS, CAS, WE, CKE output-only lines near BCM.
 - 7) Place DDR_VREF[2-1] resistor dividers near BCM.
 - 8) Trace impedances should be 60 to 65 ohms
 - 9) Route DDR_VREF[2-1] with 30-mil trace and at least 1 high quality ceramic bypass capacitor for each connection to a device.
 - 10) All traces should have a ≥ 3 to 1 spacing ratio from the reference GND/PWR layer. (e.g. 15 mil line-to-line spacing for a 5 mil dielectric thickness)

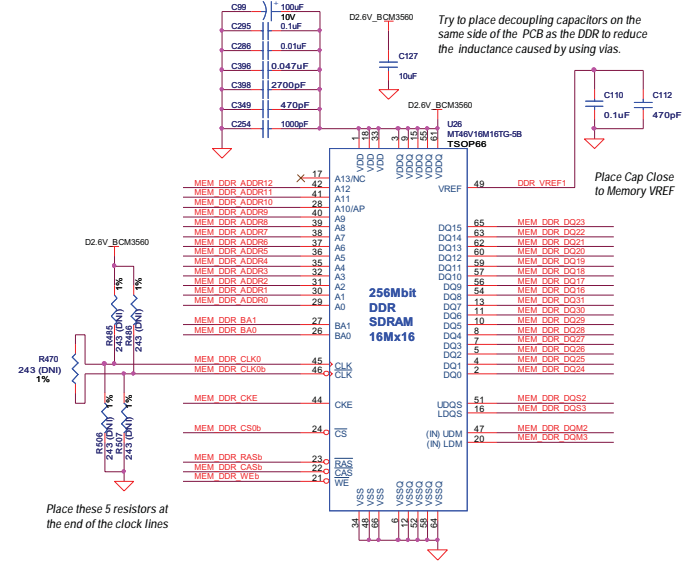


Try to place decoupling capacitors on the same side of the PCB as the DDR to reduce the inductance caused by using vias.

Place Cap Close to Memory VREF

Byte lanes swapped to optimize layout

Place these 5 resistors at the end of the clock lines



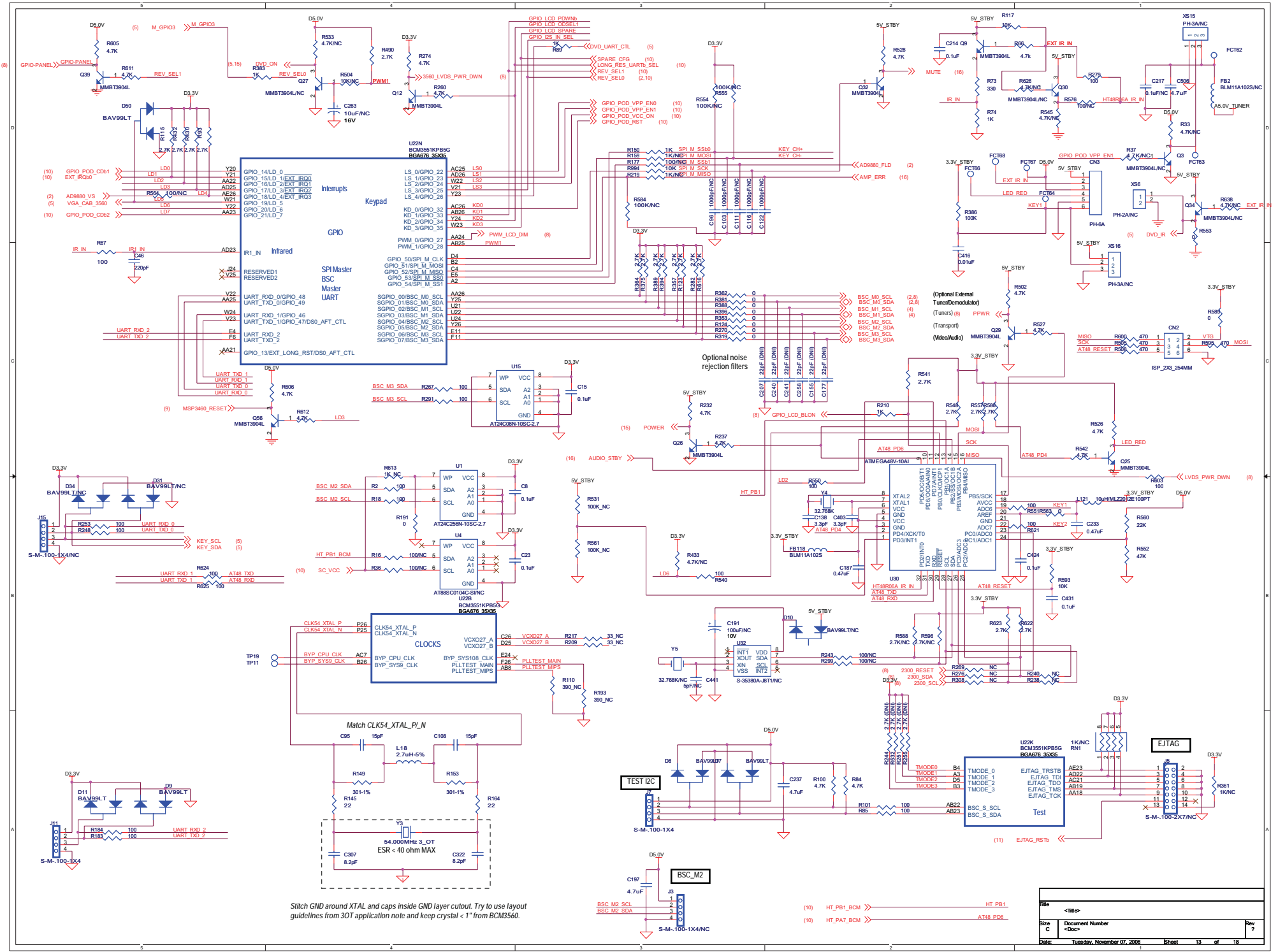
Try to place decoupling capacitors on the same side of the PCB as the DDR to reduce the inductance caused by using vias.

Place Cap Close to Memory VREF

Place these 5 resistors at the end of the clock lines

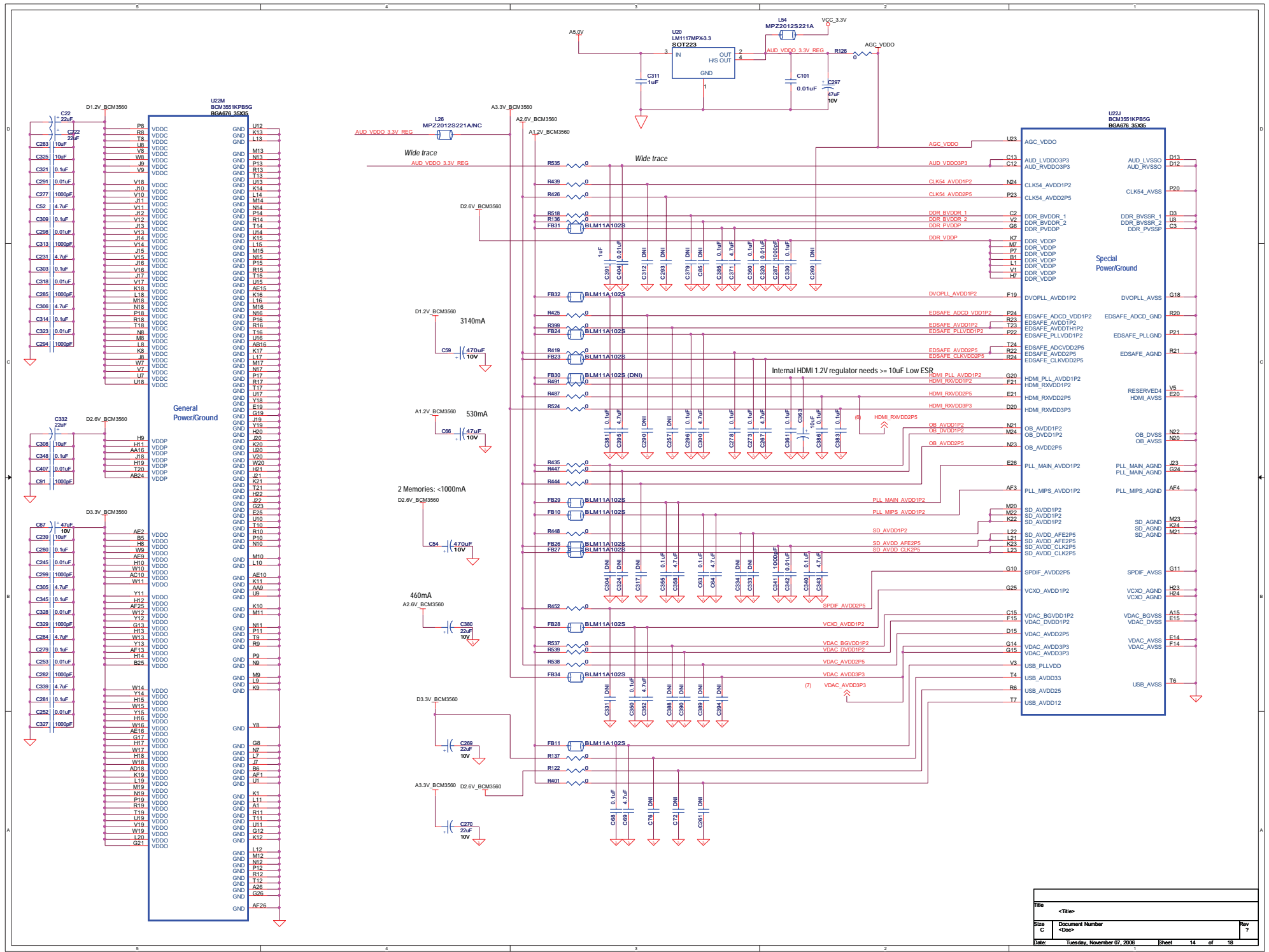
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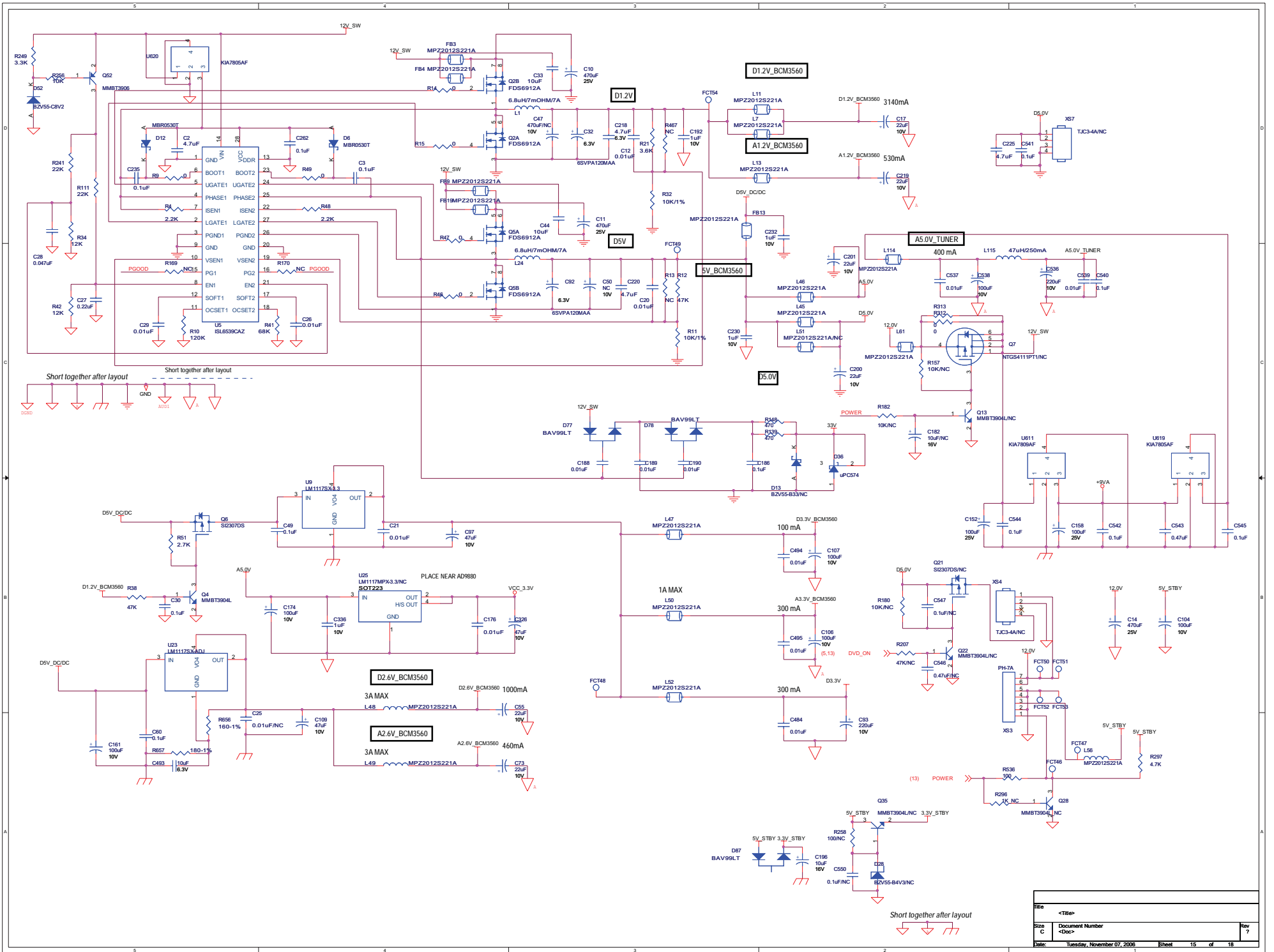


Slitch GND around XTAL and caps inside GND layer cutout. Try to use layout guidelines from 30T application note and keep crystal < 1" from BCM3560.

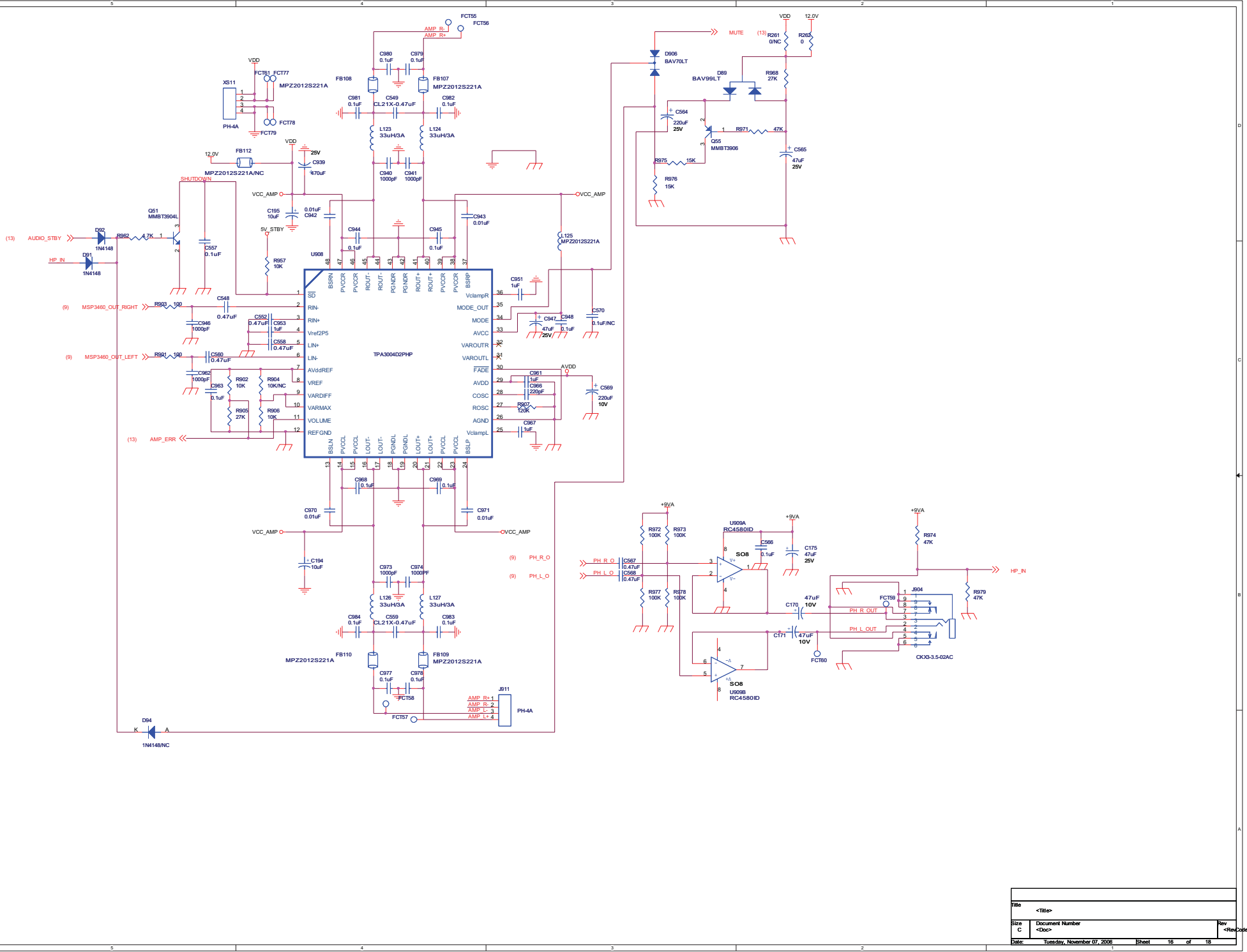
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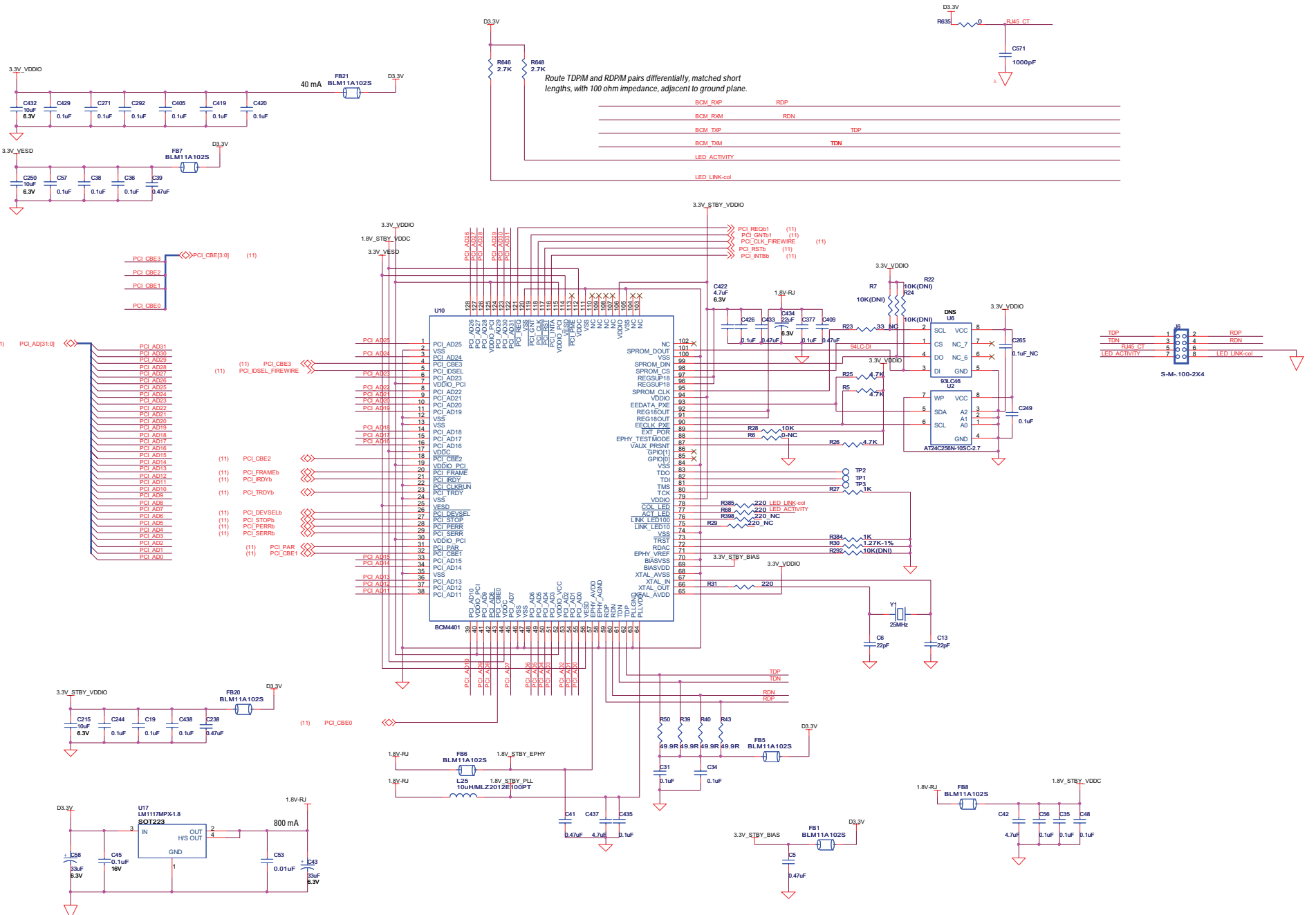
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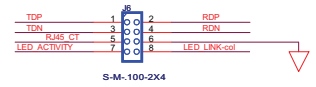
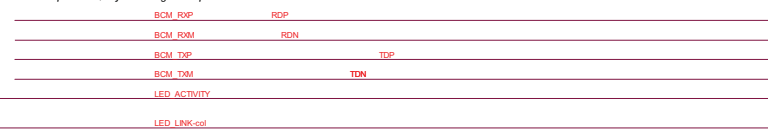
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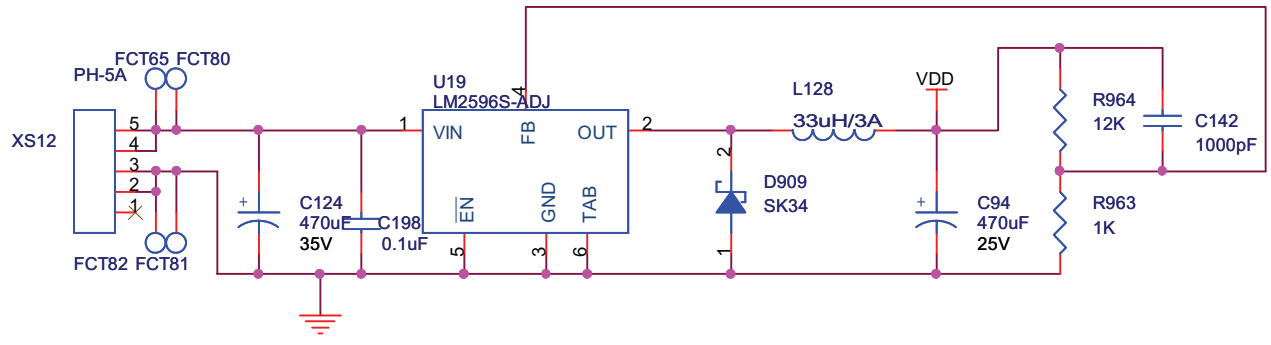
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Route TDDM and RDDM pairs differentially, matched short lengths, with 100 ohm impedance, adjacent to ground plane.



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